AF/2816 #

PATENT
Case Docket No. MICRON.113C1
Date: January 7, 2003

In re application of	:	Joseph C. Sher et al.
Appl. No.	:	09/989,563
Filed	:	November 19, 2001
For	:	CLAMP CIRCUIT WITH FUSE OPTIONS
Examiner	:	Anh Quan Tra
Art Unit	:	2816

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 2327, Washington, D.C. 20231; on

January 7, 2003
(Date)

Jerry T. Sewell
Jerry T. Sewell, Reg. No. 31,567

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BOARD OF PATENT APPEALS AND INTERFERENCES
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. Box 2327
WASHINGTON, D.C. 20231

Sir:

Transmitted herewith is an *Appellants' Brief* to the Board of Patent Appeals and Interferences.

Attached to the *Appellants' Brief are:*

Appendix A setting forth the pending claims,

Appendix B with copies of two (2) patents discussed in the Brief,

Appendix C with copies of three (3) cases cited in the brief

(X) The fee for filing a brief in the amount of $320 is enclosed.

(X) An extension of time to respond for one (1) month is hereby requested.

(X) The time extension fee for one month in the amount of $110 is enclosed.

(X) A check in the amount of $430 to cover the foregoing fees is enclosed.

(X) A return prepaid postcard.

(X) If applicant has not requested a sufficient extension of time and/or has not paid any other fee in a sufficient amount to prevent the abandonment of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 11-1410 for any fee which may be due. Please credit any overpayment to Deposit Account No. 11-1410.

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MICRON.113C1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Joseph C. Sher et al.
Appl. No.	:	09/989,563
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1/15/03
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APPELLANTS' BRIEF
PURSUANT TO 37 C.F.R. § 1.192

UNITED STATES PATENT AND TRADEMARK OFFICE
Board of Patent Appeals and Interferences
P.O. Box 2327
Arlington, Virginia 22202

Dear Sir:

Applicants (Appellants herein) appeal the final rejection of Claims 1-25 set forth in the May 31, 2001 Final Office Action. Appellants submitted a Notice of Appeal by Certificate of Mailing on October 29, 2002. According to the return postcard, the Notice of Appeal was received in the Board of Patent Appeals and Interferences on November 4, 2002. Thus, the original deadline for filing this appeal brief was January 6, 2003. This appeal brief is being submitted with a request for a one-month extension of time and the appropriate fee.

This appeal brief is filed in triplicate pursuant to 37 C.F.R. § 1.192(a). Appellants are enclosing a check in the amount of $430 to cover the $320 fee for filing an appeal pursuant to 37 C.F.R. § 1.191 and 1.17(c) and to cover the $110 fee under 37 C.F.R. § 1.136 for a one-month extension of time. Please charge any additional fees required, including any fee for an extension of time to Deposit Account No. 11-1410.

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I. REAL PARTIES IN INTEREST

The real parties in interest of the above-captioned application are:

the inventors, Joseph C Sher and Daniel R. Loughmiller; and

the assignee, Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeal or interference.

III. STATUS OF CLAIMS

The present application is a continuation of U.S. Patent Application No. 09/387,263, filed on August 31, 1999, which issued as U.S. Patent No. 6,351,180 on February 26, 2002. The present application was originally filed with Claims 1-25. Claims 1-25 of the present application generally correspond to Claims 1-9, Claims 27-32, Claim 35, and Claims 40-48 that were finally rejected and canceled in the parent application. Claims 1-25 have not been amended during prosecution of the present and are pending as originally filed on November 19, 2001. Claims 1-25 were finally rejected by the Examiner in the May 31, 2002 Final Office Action, and the final rejection was maintained in an August 27, 2002 Advisory Action. No claims have been allowed in the present application, and Claims 1-25 are the subject of this appeal.

In accordance with 37 C.F.R. § 1.192(c)(9), a copy of the set of claims involved in this appeal is included as Appendix A attached hereto.

IV. STATUS OF AMENDMENTS

As set forth in Section III, the claims have not been amended during the prosecution of the present application, and no amendment has been filed subsequent to the final rejection.

V. SUMMARY OF APPELLANTS' INVENTION

This invention relates generally to a voltage regulation circuit in a semiconductor device. Such a voltage regulation circuit is used, for example, to generate a regulated constant supply

voltage within a dynamic random access memory (DRAM) to enable certain portions of the DRAM circuitry to operate at a higher voltage than the external supply voltage provided as an input to the DRAM. (*See*, paragraph 0005 on page 2 of the specification.) As further described in the specification, during the testing of the DRAM circuitry by the manufacturer, it is often desirable to increase the regulated constant supply voltage generated within the DRAM to ensure that the device is operating properly. (*See*, paragraph 0007 on page 2 of the specification.) On the other hand, after a DRAM circuit is delivered to a customer, a test performed on a DRAM at a higher voltage may fail because the customer may not control the testing conditions as well as the manufacturer. (*See*, paragraph 0007 on page 2 of the specification.)

An object of this invention is to generate a higher regulated constant supply voltage for use during testing of the DRAM by the manufacturer but to limit the voltage level generated within the DRAM once the manufacturer's tests are completed and the DRAM has been shipped to a customer. This prevents the customer from inadvertently damaging the DRAM by generating the higher voltage when the testing environment is not properly controlled. (*See*, paragraph 0008 on page 3 of the specification.)

VI. ISSUE PRESENTED ON APPEAL

The following issue is presented on appeal:

Whether Appellants' claimed inventions should be deemed obvious where the cited references do not teach or suggest the claimed subject matter.

VII. GROUPING OF CLAIMS

For the purposes of this appeal only, Appellants group the pending claims as follows:

Group I: Claims 1-9, 15, 16 and 25

Group II: Claims 10-14

Group III: Claims 17-24

VIII. ARGUMENT

For the Board's convenience, Appellants are including copies of the references discussed herein in Appendix B, and copies of the cases relied upon herein in Appendix C.

A. DISCUSSION OF THE REFERENCES RELIED UPON BY EXAMINER

In the Final Office Action, the Examiner rejects Claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,483,486 to Javanifard et al. in view of U.S. Patent No. 5,473,277 to Furumochi.

Javanifard et al.

U.S. Patent No. 5,483,486 to Javanifard et al. ("Javanifard") discloses a charge pump circuit for providing multiple output voltages to a flash memory. The charge pump in Javanifard boosts an input supply voltage to a higher voltage required by a circuit such as a flash electrically erasable programmable read only memory (flash EEPROM). Javanifard utilizes a multiplexor connected to first and second regulation circuits to selectively control a single charge pump to output a first output voltage or a second output voltage in accordance with the regulation circuit coupled to the charge pump via the multiplexor.

Furumochi

U.S. Patent No. 5,473,277 to Furumochi discloses an output circuit for providing a finely adjustable voltage. Furumochi includes a constant voltage generator circuit that uses a ROM fuse circuit that is programmed to generate an external control signal. The external control signal is used to adjust the back-gate voltages of a plurality of series connected transistors that have their respective gates and drains connected together. By varying the back-gate voltages of the transistors, the threshold voltages of the transistors are varied such that the total voltage across the transistors is varied to enable the constant output voltage to be finely adjusted.

B. DISCUSSION OF THE ISSUE ON APPEAL

Appellants' claimed inventions are not obvious because the cited references do not teach or suggest the claimed subject matter.

The Examiner asserts that Javanifard discloses a circuit comprising a reference circuit, a voltage regulator electrically coupled to the reference circuit which generates a first control signal, and a charge pump that receives the control signal and generates a test supply voltage. Therefore, the Examiner asserts that Javanifard shows all elements of Claim 1 except for the reference circuit having a plurality of voltage regulation devices and having at least one bypass device connected to at least one of the plurality of voltage regulation devices. Furthermore, the Examiner states that Figure 5 of Furumochi shows "a reference circuit having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices." The Examiner also states that "it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifard et al.'s reference circuit for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump." Moreover, the Examiner states that with the combination, it is inherent that the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

For the reasons set forth below for each of the three groups of claims, Appellants respectfully disagree with the Examiner's analysis and conclusions. Appellants respectfully submit that all pending claims are patentably distinguished over the cited references.

Group I: Claims 1-9, 15, 16 and 25

Appellants respectfully submit that the Examiner has not established a *prima facie* case of obviousness as to Claim 1 because: (1) the cited references, individually or in combination, do not teach or suggest every feature of Claim 1; and (2) there is no suggestion or motivation to

combine or modify the cited references in a way that would make Claim 1 obvious in view of the prior art.

Claim 1 is directed to a voltage control circuit comprising, among other elements, a clamp circuit having a plurality of voltage regulation devices that control a clamping threshold of the clamp circuit. The term "clamp circuit," as would be understood by one with ordinary skill in the relevant art, describes a circuit that operates to place a limit on (or to clamp) a signal if the signal reaches a certain predetermined value. This limiting, or clamping, does not occur until the signal reaches the predetermined value, and the signal is allowed to vary until that point. This understanding of the term "clamp circuit" is also supported by the surrounding claim language of Claim 1. Claim 1 recites this limit controlled by the clamp circuit as the "clamping threshold." As appreciated by one with ordinary skill in the relevant art, and consistent with the understanding of a clamp circuit, the term "clamping threshold" corresponds to a limit placed on a signal wherein some action occurs when the signal reaches that limit. Thus, the clamp circuit of Claim 1 operates to place a limit on a signal when that signal reaches a certain predetermined level. This limit on the voltage signal corresponds to the clamping threshold of the clamp circuit and ensures that the safe operating voltage of the charge pump is not exceeded.

Neither Javanifard nor Furumochi teaches or suggests a voltage control circuit comprising a clamp circuit having a clamping threshold. Javanifard discloses a circuit for generating a desired output voltage (see column 19, line 16). With reference to Figure 14, Javanifard shows a supply circuit having, among other elements, a reference circuit. This voltage reference circuit is disclosed as using an input voltage to generate a reference voltage. Nowhere in the specification or in the depicted embodiments does Javanifard teach or suggest a voltage control circuit having a clamp circuit or a circuit having a clamping threshold. In particular, the reference voltage is fixed such that it does not vary above or below the desired voltage.

Like Javanifard, Furumochi does not teach or suggest a voltage control circuit having a clamp circuit. Furumochi describes in column 2 at lines 59-60 that its invention relates to a voltage generator circuit for generating "constant voltages in fine steps." Referring to the preferred embodiment of the invention depicted in Figure 5, Furumochi describes the constant

voltage generator as being designed for supplying a constant voltage with "strict precision" (see column 7, lines 16-17). The voltage supplied by the Furumochi circuit is kept fixed, as noted by the Examiner, and is not allowed to vary above or below the voltage selected by the diode-configured transistors that are not bypassed. To assert that Furumochi teaches or suggests a clamp circuit not only goes against the accepted meaning of the term, but also ignores other express limitations of Claim 1, including the limitation of a "clamping threshold." Furumochi does not teach a circuit that allows an output signal to vary up to a clamping threshold. Rather, once the selected diode-configured transistors are bypassed in Furumochi, the output signal is fixed and does not vary above or below the selected output voltage. Thus, Furumochi, in combination with Javanifard, does not render obvious the embodiment of the present invention recited in Claim 1, which includes a clamp circuit having a clamping threshold. See M.P.E.P. § 2143.03 (all words in claim must be considered in judging the patentability of that claim against prior art).

In addition to reciting a voltage control circuit having a clamp circuit, Claim 1 also recites the voltage control circuit having at least one bypass device that is activated following certification of the semiconductor device to bypass at least one of a plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit. This lower clamping threshold limits the supply voltage of the semiconductor device and prevents the customer from subsequently testing the semiconductor device using harmful voltage levels.

Neither Javanifard nor Furumochi recites a voltage control circuit that comprises a bypass device that is activated following the certification of a semiconductor device to bypass at least one of a plurality of voltage regulation devices to lower the clamping threshold of a clamp circuit. Rather, Furumochi discloses a constant voltage generator having a switching element (SW0) comprising an n-type transistor connected at its gate to a ROM fuse circuit via an inverter (see column 7, lines 45-50). This switching element, however, cannot be activated to bypass a voltage regulation device in order to lower a clamping threshold. Specifically, the switching element taught by Furumochi may operate either in an "ON" state or an "OFF" state. When in an "ON" state, the switching element bypasses a transistor T4 and causes the output voltage of the

voltage generator circuit be at a lower level. When in an "OFF" state, the switching element does not bypass the transistor T4 and causes the output voltage of the voltage regulator to be at a higher level (see Table 1). However, the switching element disclosed by Furumochi may not "switch" from the "OFF" state (higher output voltage) to the "ON" state (lower output voltage). This is because, to be in the "OFF" state, fuse elements of the ROM fuse circuit in the switching element are melted and disconnected (see, for example, column 9, lines 22-33). In other words, the "OFF" state, which results in a higher output voltage produced by the voltage generator circuit, is permanent, and the switching element cannot subsequently be activated (or switched to an "ON" state) to lower the output voltage of the voltage generator circuit. Thus, neither of the cited references discloses a bypass device that may be activated to lower the clamping threshold of a clamp circuit.

Furthermore, there is no suggestion or motivation to combine or to modify the references that would make Claim 1 obvious to one of ordinary skill in the art. Javanifard and Furumochi, individually or in combination, teach away from the claimed invention. Both Figure 14 of Javanifard and Figure 5 of Furumochi disclose reference circuits. In particular, the reference circuit disclosed in Furumochi is designed to generate a fixed reference voltage. Such a high precision reference circuit for producing a fixed reference voltage teaches away from the use of a clamp circuit that allows an output signal to vary below a clamping threshold. Because Furumochi teaches away from the present invention, Appellants submit that there is no suggestion or motivation to combine Javanifard and Furumochi in a way to render the present invention obvious.

On pages 4-5 of the May 31, 2002 Final Office Action, the Examiner states that Appellants' arguments submitted in response to the first Office Action were fully considered but are not persuasive. In particular, and in response to the Appellants' argument that the cited references do not teach a clamp circuit, the Examiner states:

> [I]t is well known that diode works as a clamp. The diodes in Furumochi's circuits forcing the output node to a fix voltage. Therefore, Furumochi's reference circuit can be considered as clamp circuits. . . . Furthermore, it is seen as inherent for the supply voltage to be vary. That why the diodes is used in the

circuit for the purpose of generating a fix reference voltage when the supply voltage exceed the threshold voltages of the diodes.

Appellants agree with the Examiner that, under certain conditions, a diode may work as a clamping device. However, it is well known to one of ordinary skill in the relevant art that a circuit containing a diode, or other clamping device, is not necessarily a clamp circuit. As set forth above, neither Furumochi nor Javanifard teaches or suggests the use of a clamping circuit. Even though Furumochi discloses the use of diode-configured transistors in its voltage reference circuit depicted in Figure 5, Furumochi never discloses or suggests a clamp circuit having a clamping threshold.

As discussed above, the "high-precision" voltage reference circuit of Furumochi teaches away from the claimed invention, which comprises a clamping circuit that allows an output voltage to vary up to a clamping threshold. If the reference circuit of Furumochi were designed to function as a clamping circuit with a clamping threshold, as the Examiner's statement suggests, the reference circuit of Furumochi would be rendered unsatisfactory for its intended purpose of supplying a "high precision" constant reference voltage. Such a modification of Furumochi's disclosure is improper and is not sufficient to establish a *prima facie* case of obviousness. *See* M.P.E.P. § 2143.01 (proposed modification cannot render prior art unsatisfactory for its intended purpose and cannot change the principal of operation of the prior art invention). *See also, In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984); and *In re Ratti*, 270 F.2d 810, 813, 123 USPQ 349, 352 (C.C.P.A. 1959).

For the foregoing reasons, Appellants respectfully submit that Claim 1 is patentably distinguished over Javanifard and Furumochi. The Examiner's rejection of Claim 1 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Appellants respectfully submit that independent Claims 4, 15 and 25 are patentably distinguished over Javanifard and Furumochi for the reasons set forth above and for the different features recited in each of the independent claims. The Examiner's rejection of Claims 1, 4, 15, and 25 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Claims 2-3 and 6-9 depend from Claim 1 and further define the invention defined in Claim 1. Claim 5 depends from Claim 4 and further defines the invention defined in Claim 4. Claim 16 depends from Claim 15 and further defines the invention defined in Claim 15. In view of the foregoing remarks regarding the patentability of Claims 1, 4 and 15, Appellants respectfully submit that dependent Claims 2-3, 5-9 and 16 are also patentably distinguished over the cited references. The Examiner's rejection of Claims 2-3, 5-9 and 16 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Group II: Claims 10-14

Claim 10 is an apparatus claim defined with "means plus function" limitations. Although the Examiner states that "Claims 10-21 and 25 recite similar limitations of claims 1-9" and rejects those claims "for the same reasons," Appellants respectfully submit that Claim 10 and dependent Claims 11-14 are separately patentable from the claims in Groups I and III because the means plus functions limitations in Claims 11-14 must be examined in accordance with the guidelines set forth in M.P.E.P. §§ 2181-2186.

Claim 10 recites a voltage control circuit comprising, among other elements, means for controlling an output of a clamp circuit. As previously discussed, neither Javanifard nor Furumochi discloses or suggests a voltage control circuit having a clamp circuit. Furthermore, there is no suggestion in either reference of a means for generating a first control signal based upon the output of the clamp circuit, a means for generating a test supply voltage, a means for limiting the output of the clamp circuit, means for generating a second control signal, and a means for generating an operational supply voltage. The Examiner's stated basis for the rejection does not indicate where the foregoing combination of elements can be found in the two references. Thus, Appellants respectfully submit that Claim 10 is patentably distinguished over the cited references. Appellants respectfully submit that the Examiner's rejection of Claim 10 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Claims 11-14 depend from Claim 10 and further define the invention defined in Claim 10. In view of the foregoing remarks regarding the patentability of Claim 10, Appellants respectfully submit that dependent Claims 11-14 are also patentably distinguished over the cited references. The Examiner's rejection of Claims 11-14 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Group III: Claims 17-24

Claims 17-24 are claims directed to a method of providing a first voltage supply on a semiconductor device during a first period and a second supply voltage during a second period. Since the limitations of Claims 17-24 are functional limitations rather than structural limitations, Claim 17-24 are separately patentable from the structural claims of Group I and the means plus function claims of Group II.

The method of Claim 17 comprises, among other steps, generating the first supply voltage from a first voltage control signal, reversibly bypassing at least one of a plurality of voltage control elements, and generating the second supply voltage from a second voltage control signal that is established from the plurality of voltage control elements which are not reversibly bypassed.

Furumochi does not teach or suggest a method comprising the step of reversibly bypassing at least one of a plurality of voltage control elements. Rather, Furumochi discloses a switching element (SW0) wherein the gate of a transistor is connected to a ROM fuse circuit (see, for example, column 7, lines 45-50). In particular, the ROM fuse circuit of Furumochi comprises a resistor and a fuse element connected in series between a power source and a ground line (see column 8, lines 19-24). As previously discussed with respect to Claim 1, the "OFF" state of switching element SW0 is permanent because the fuse elements of the ROM fuse circuit are melted and disconnected to make the state "concrete" (see, for example, column 9, lines 22-33). Thus, the "OFF" state of the switching element SW0 is not reversible, and the switching element cannot reversibly bypass a voltage control element in order to establish a second voltage

control signal. Nowhere does Furumochi teach or suggest the step of reversibly bypassing at least one of the plurality of voltage control elements.

The Examiner also asserts in the last paragraph on page 5 of the May 31, 2002 Final Office Action that:

> In response for the arguments of claim 17, Furumochi's figure 4 shows the step of generating the first supply voltage (Vout when switch 11A opened) from the first control signal and reversibly bypassing at least one of the plurality of the voltage control elements (by switch 11A) which are not reversibly bypass, a second supply voltage (Vout when switch 11a closed) from the second control signal.

Appellants note that Figure 4 of Furumochi does not show a switch 11A, and Appellants assume that the Examiner's statement is intended to be directed to Figure 3 on the same page. Appellants also respectfully submit, in light of the remarks made above, that Furumochi's Figure 3 does not teach the step of reversibly bypassing at least one of a plurality of voltage control elements in order to establish a second voltage control signal. The Examiner's statement appears to be reading an element into Figure 3 that is not disclosed by Furumochi. When reading Figure 3 with the corresponding specification and subsequent figures, one with ordinary skill in the relevant art would understand the switching 11A of Figure 3 to be controlled by the ROM fuse circuit. Once the switching element 11A is opened (to not bypass transistor Tn), the switching element may not subsequently be closed because the open, or "OFF," state is permanent due to the configuration of the ROM fuse circuit. To open switching element 11A, Furumochi teaches that the fuse elements of the ROM fuse circuit are melted and disconnected, which creates an irreversible open state. Thus, Appellants submit that Figure 3, in view of the corresponding specification, does not disclose each step of Claim 17.

Because Claim 17 includes elements not taught or suggested by Javanifard or Furumochi, Appellants respectfully submit that Claim 17 is patentably distinguished over the two references. The Examiner's rejection of Claim 17 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Claims 18-24 depend from Claim 17 and further define the invention defined in Claim 17. In view of the foregoing remarks regarding the patentability of Claim 17, Appellants

respectfully submit that dependent Claims 18-24 are also patentably distinguished over the cited references. The Examiner's rejection of Claims 18-24 under 35 U.S.C. § 103(a) is not supported by the cited references and should be reversed by the Board.

Summary of Arguments

As set forth above for each of the three groups of claims, the final rejection of the claims under 35 U.S.C. § 103(a) as being unpatentable over Javanifard in view of Furumochi should be reversed because neither reference teaches or suggests the claimed subject matter to those of ordinary skill in the art, and the Examiner fails to show how the teachings of the two references can be combined to disclose or suggest the claimed subject matter. In particular, the Examiner's conclusory statements forming the basis for the rejection under 35 U.S.C. § 103(a) do not meet the standards set forth in a recent decision of the Court of Appeals for the Federal Circuit in *In re Lee*, 277 F.3d 1338, 134361 USPQ2d 1430, 1434 (Fed. Cir. 2002):

> The examiner's conclusory statements . . . do not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Thus the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion.

Under the well-established law reiterated by the Court of Appeals for the Federal Circuit in *In re Lee*, in order for the Examiner to properly reject claimed subject matter of the present application, the Examiner must cite references that teach the subject matter and must form arguments based on the combined teachings of the references as a basis for the rejection. Furthermore, the Examiner must show some suggestion to combine the references. The Examiner has not met that burden in the final rejection of the claims of the present application. Therefore the final rejection should be reversed as to all claims.

IX. CONCLUSION

Appellants' respectfully submit that the claims pending in the present application are patentably distinguished over Javanifard in view of Furumochi. Appellants' respectfully request that this Board overturn the Examiner's rejections and to remand this application to the Examiner with directions to pass all pending claims to allowance.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: JANUARY 7, 2003 By: Jerry T. Sewell

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APPENDIX A

Claims Presented on Appeal

1. A voltage control circuit which provides a test supply voltage during manufacturing and testing of a semiconductor device and an operational supply voltage after certification of the semiconductor device, the operational supply voltage being lower than the test supply voltage, the voltage control circuit comprising:

a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit;

a voltage regulator electrically coupled to the clamp circuit which generates a first control signal responsive to the clamping threshold of the clamp circuit;

a charge pump which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage; and

at least one bypass device connected to at least one of the plurality of voltage regulation devices, wherein the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the

voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

2. The voltage control circuit of Claim 1, wherein the plurality of voltage regulation devices comprise diodes.

3. The voltage control circuit of Claim 2, wherein the diodes are implemented through transistors.

4. A voltage control circuit which provides a test supply voltage during manufacturing and testing of a semiconductor device and an operational supply voltage after certification of the semiconductor device, the operational supply voltage being lower than the test supply voltage, the voltage control circuit comprising:

a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit;

a voltage regulator electrically coupled to the clamp circuit which generates a first control signal responsive to the clamping threshold of the clamp circuit;

a charge pump which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage; and

at least one bypass device connected to at least one of the plurality of voltage regulation devices, the bypass device comprising a fuse in series with a transistor, wherein the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

5. The voltage control circuit of Claim 4, wherein bypass device is activated by blowing the fuse.

6. The voltage control circuit of Claim 1, wherein value of the operational supply voltage is reduced for each voltage regulation device bypassed.

7. The voltage control circuit of Claim 1, wherein the voltage regulation devices limit the maximum voltage output of the clamp circuit.

8. The voltage control circuit of Claim 1, wherein the first control signal reduces the test supply voltage when the voltage regulation devices limit the output of the clamp circuit.

9. The voltage control circuit of Claim 1, wherein the second control signal reduces the operational supply voltage when the non-bypassed voltage regulation devices limit the output of the clamp circuit.

10. A voltage control circuit which provides a test supply voltage during manufacturing and testing of a semiconductor device and an operational supply voltage after certification of the semiconductor device, the operational supply voltage being lower than the test supply voltage, the voltage control circuit comprising:

means for controlling an output of a clamp circuit;

means for generating a first control signal based upon the output of the clamp circuit;

means for generating the test supply voltage;

means for limiting the output of the clamp circuit;

means for generating a second control signal based upon the limited output of the clamp circuit; and

means for generating the operational supply voltage.

11. The voltage control circuit of Claim 10, wherein the control means comprise diodes.

12. The voltage control circuit of Claim 11, wherein the diodes are implemented through transistors.

13. The voltage control circuit of Claim 10, wherein the limiting means comprises a fuse.

14. The voltage control circuit of Claim 10, wherein the limiting means comprises a transistor.

15. A voltage control circuit comprising:

a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit;

a voltage regulator electrically coupled to the clamp circuit, the voltage regulator generating a control signal responsive to the clamping threshold of the clamp circuit;

a charge pump electrically coupled to the voltage regulator, the charge pump generating a voltage in response to the control signal from the voltage regulator; and

at least one bypass device connected to at least one of the plurality of voltage regulation devices, wherein the at least one bypass device is reversibly activated to reversibly bypass the at least one of the plurality of voltage regulation devices from the clamp circuit, thereby modifying the clamping threshold of the clamp circuit.

16. The voltage control circuit of Claim 15, wherein the bypass device comprises a fuse in series with a control terminal of a transistor.

17. A method of providing a first supply voltage on a semiconductor device during a first period and a second supply voltage during a second period, the method comprising the steps of:

providing a plurality of voltage control elements;

establishing a first voltage control signal from the voltage control elements;

generating the first supply voltage from the first voltage control signal;

reversibly bypassing at least one of the plurality of voltage control elements;

establishing a second voltage control signal from the plurality of voltage control elements which are not reversibly bypassed; and

generating the second supply voltage from the second voltage control signal.

18. The method of Claim 17, wherein the first supply voltage has a voltage magnitude greater than the second supply voltage.

19. The method of Claim 17, wherein the plurality of voltage control elements comprise diodes.

20. The method of Claim 17, wherein reversibly bypassing at least one of the plurality of voltage control elements comprises applying a control signal to a bypass device.

21. The method of Claim 17, wherein the first supply voltage and the second supply voltage are generated by a charge pump.

22. The method of Claim 17, further comprising:

irreversibly bypassing at least one of the plurality of voltage control elements;

establishing a third voltage control signal during a third period from the plurality of voltage control elements which are not irreversibly bypassed; and

generating a third supply voltage from the third voltage control signal.

23. The method of Claim 22, wherein irreversibly bypassing at least one of the plurality of voltage control elements comprises blowing a fuse.

24. The method of Claim 22, wherein the at least one of the plurality of voltage control elements are irreversibly bypassed after testing of the semiconductor device.

25. A voltage control circuit for a semiconductor device, the voltage control circuit generating an internal supply voltage within the semiconductor device, the internal supply voltage derived from an external supply voltage that varies over a range of magnitudes, the voltage control circuit comprising:

a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit;

a voltage regulator electrically coupled to the clamp circuit which generates a first control signal responsive to the clamping threshold of the clamp circuit;

a charge pump which receives the control signal from the voltage regulator, the charge pump generating the internal supply voltage from the external supply voltage, the internal supply voltage varying in response to changes in the magnitude of the external supply voltage and having a magnitude greater than the magnitude of the external supply voltage by a differential magnitude responsive to the clamping threshold of the clamp circuit; and

at least one bypass device connected to at least one of the plurality of voltage regulation devices, wherein the at least one bypass device is activated following testing of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the internal supply voltage at an operational magnitude having a reduced differential magnitude with respect to magnitude of the external supply voltage.

APPENDIX B

Copies of References Discussed in Appeal Brief

Copies of the following references are attached hereto:

U.S. Patent No. 5,473,277 to Furumochi, issued on December 5, 1995, for *Output Circuit for Providing a Finally Adjustable Voltage*.

U.S. Patent No. 5,483,486 to Javanifard et al., issued on January 9, 1996, for *Charge Pump Circuit for Providing Multiple Output Voltages for Flash Memory*.

US005473277A

United States Patent [19]

Furumochi

[11] Patent Number: 5,473,277

[45] Date of Patent: Dec. 5, 1995

[54] **OUTPUT CIRCUIT FOR PROVIDING A FINALLY ADJUSTABLE VOLTAGE**

[75] Inventor: **Kazuto Furumochi**, Nakahara, Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **222,943**

[22] Filed: **Apr. 5, 1994**

[30] **Foreign Application Priority Data**

May 13, 1993 [JP] Japan 5-111748

[51] **Int. Cl.**[6] **G05F 1/10**

[52] **U.S. Cl.** **327/543**; 327/538; 327/537; 365/189.09

[58] **Field of Search** 327/362, 538, 327/543, 401, 378, 535, 537, 534; 365/189.09

[56] **References Cited**

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4,899,309	2/1990	Kitazawa et al.	365/189.09
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5,099,146	3/1992	Miki et al.	327/537

Primary Examiner—Timothy P. Callahan
Assistant Examiner—Jung Ho Kim
Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram

[57] **ABSTRACT**

A constant voltage generator circuit comprises adjusting means for making fine adjustment of each back-gate voltage of transistors on the basis of external control signals, and a transistor circuit for outputting a constant voltage adjusted on the basis of the back-gate voltage. A constant voltage generator circuit comprises adjusting means for making fine adjustment of each back-gate voltage of transistors on the basis of external control signals; and a transistor circuit for outputting a constant voltage adjusted on the basis of the back-gate voltages, the transistor circuit including a plurality of N transistors with their respective gates and sources connected together, and a load element for dividing the power source voltage with a plurality of N transistors. Adjusting means comprises a plurality of N-1 switching circuits for supplying bias voltages individually to the back-gate of the first through (N-1)th transistors in the transistor circuit on the basis of the external control signal, and a switching element for stopping the operation of the Nth transistor in the transistor circuit on the basis of the external control signal. A semiconductor memory comprises memory means for storing information; and constant voltage generating means for supplying voltage to memory means, the constant voltage generating means including adjusting means for making fine adjustment of each back-gate voltage of a plurality of transistor on the basis of external control signals, and a transistor circuit for outputting the constant voltage adjusted on the basis of the back-gate voltages.

12 Claims, 10 Drawing Sheets

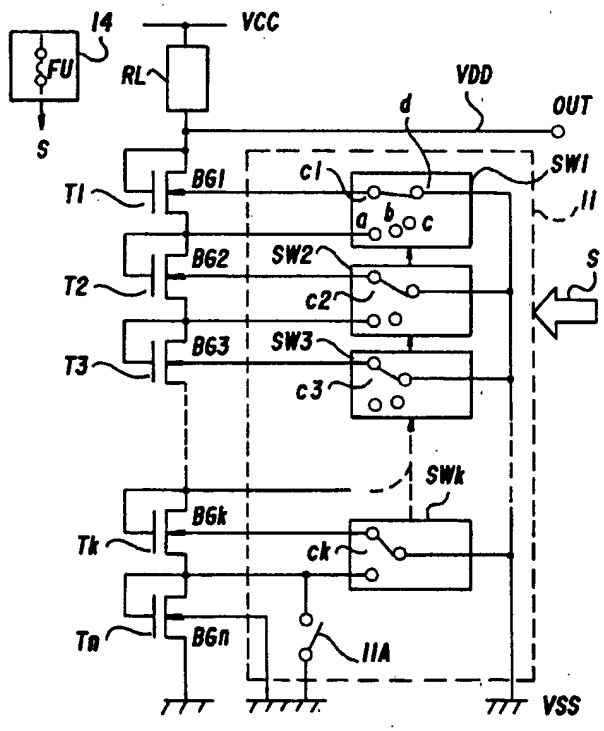


FIG.2
PRIOR ART

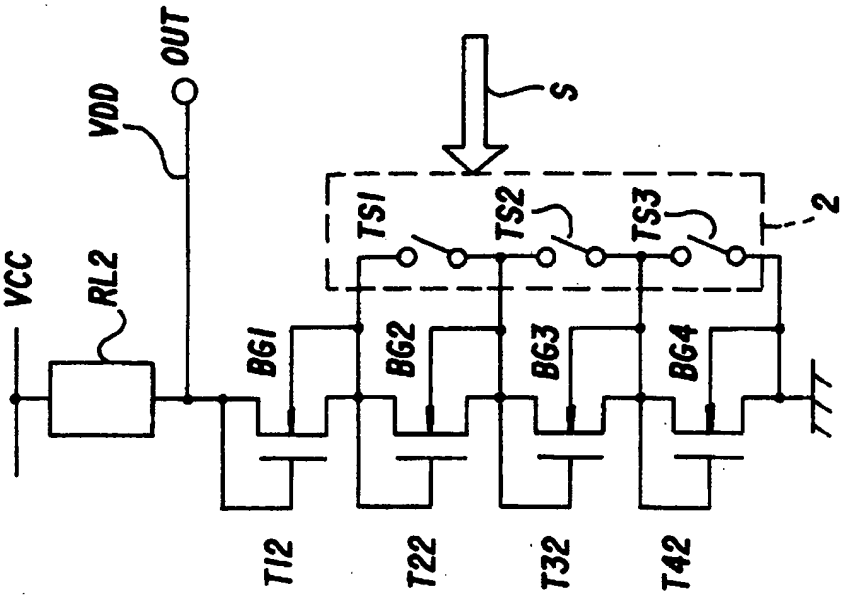


FIG.1
PRIOR ART

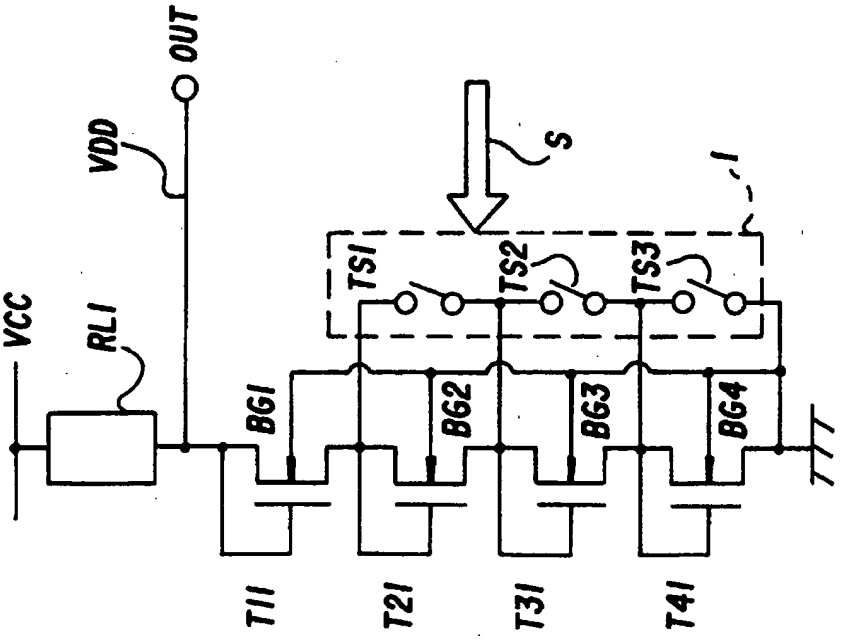
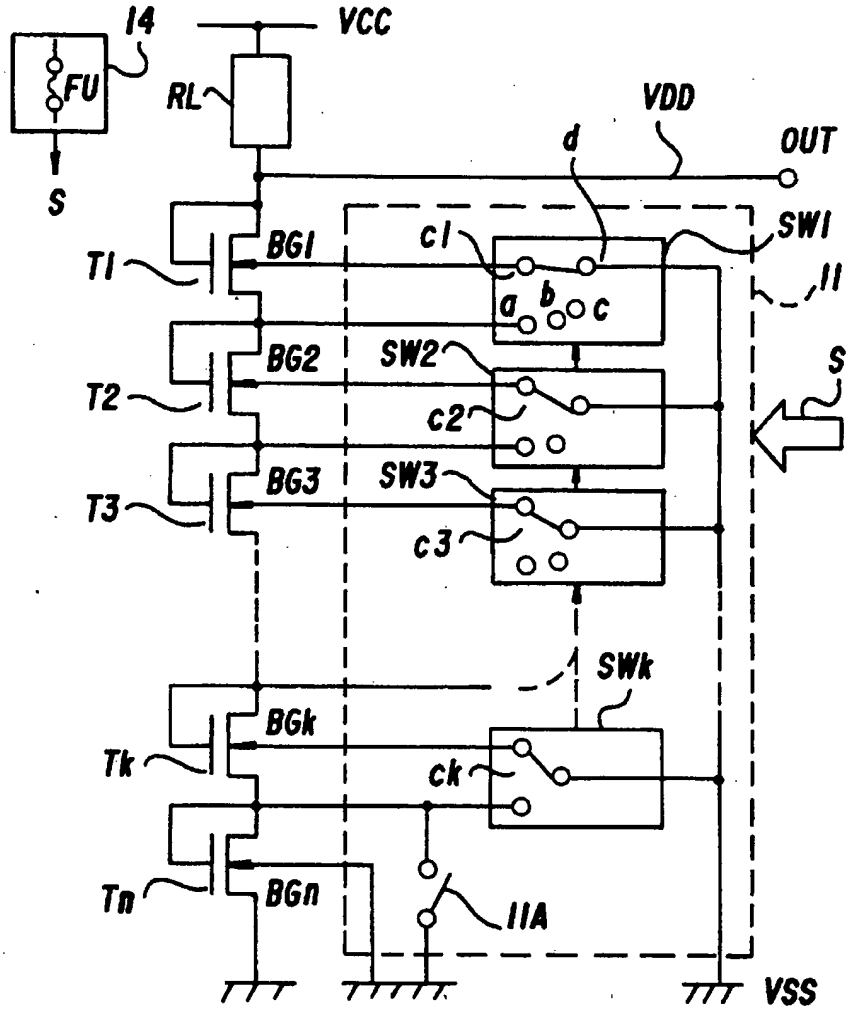


FIG.3


14
VCC
FU
RL
VDD
d
OUT
S
BG1
c1
SW1
T1
11
a
b
c
BG2
SW2
S
T2
c2
BG3
SW3
T3
c3
SWk
BGk
Tk
ck
Tn
BGn
11A
VSS

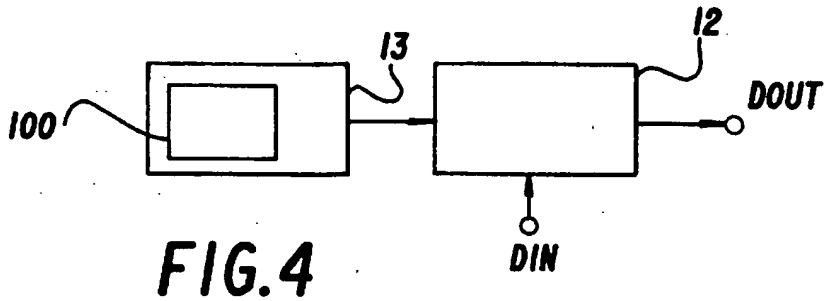
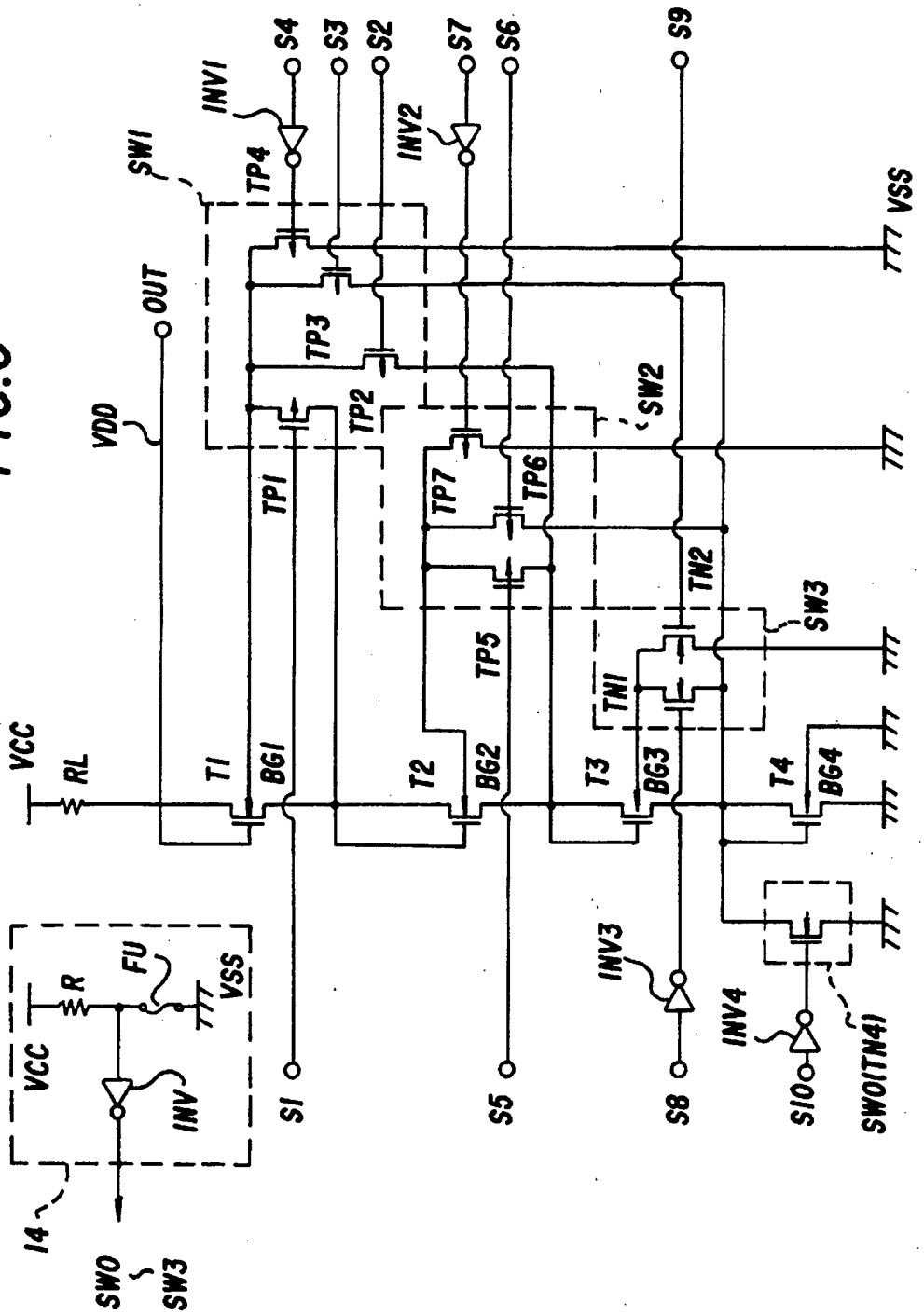

13
12
100
DOUT
DIN

FIG.4

FIG.5


S4
S3
S2
S7
S6
S9
INV1
INV2
SW1
TP4
VSS
OUT
TP3
SW2
VDD
TP2
TP1
TP7
TP6
TN2
SW3
TP5
TN1
VCC
RL
T1
BG1
T2
BG2
T3
BG3
T4
BG4
INV3
INV4
R
FU
VSS
VCC
INV
S1
S5
S8
S10
SW0(TN4)
I4
SW0
SW3

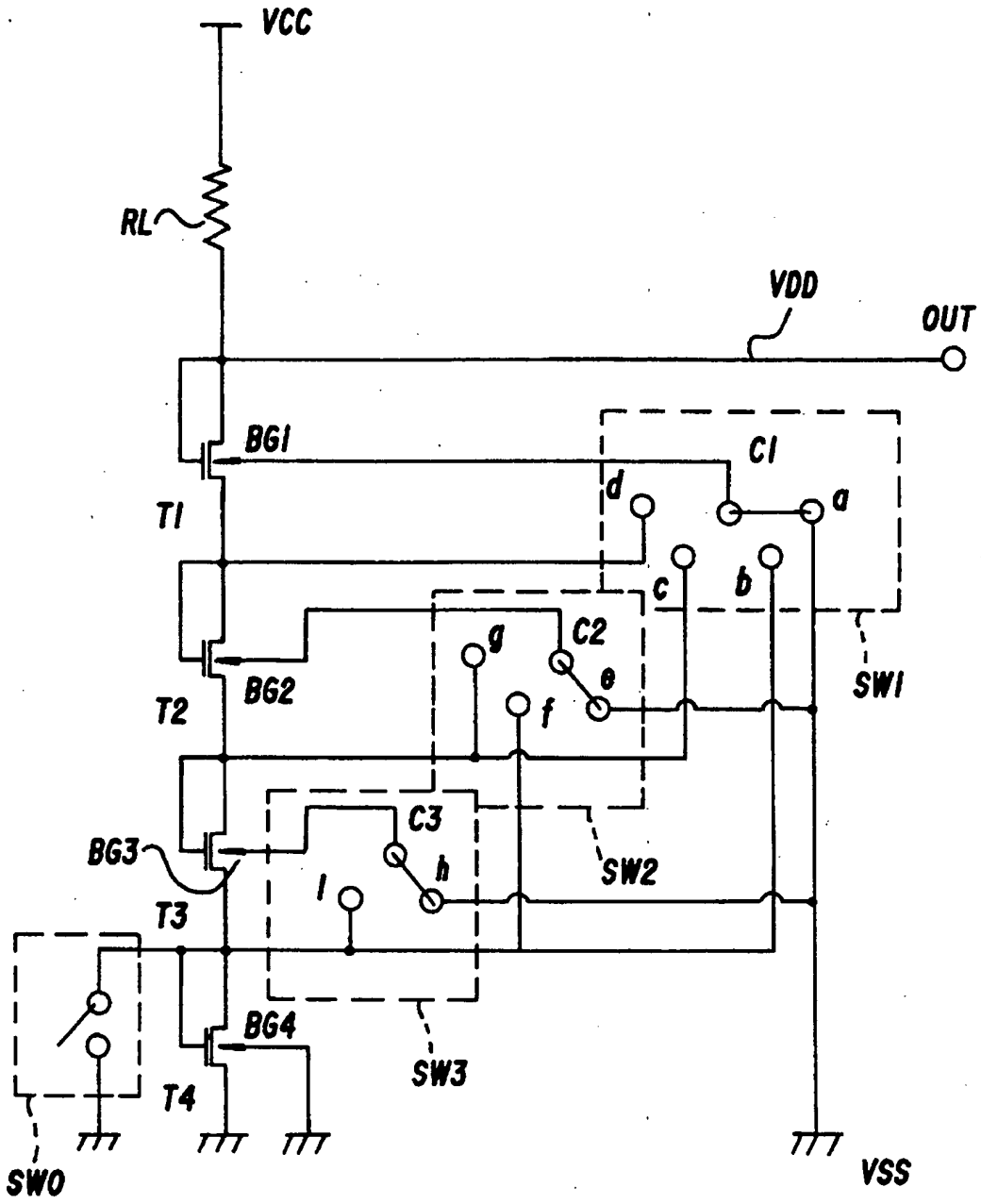

VCC
RL
VDD
OUT
BG1
C1
d
a
T1
c
b
g
C2
e
BG2
SW1
T2
f
C3
BG3
h
SW2
l
T3
BG4
SW3
T4
SW0
VSS

FIG.6

FIG. 7B

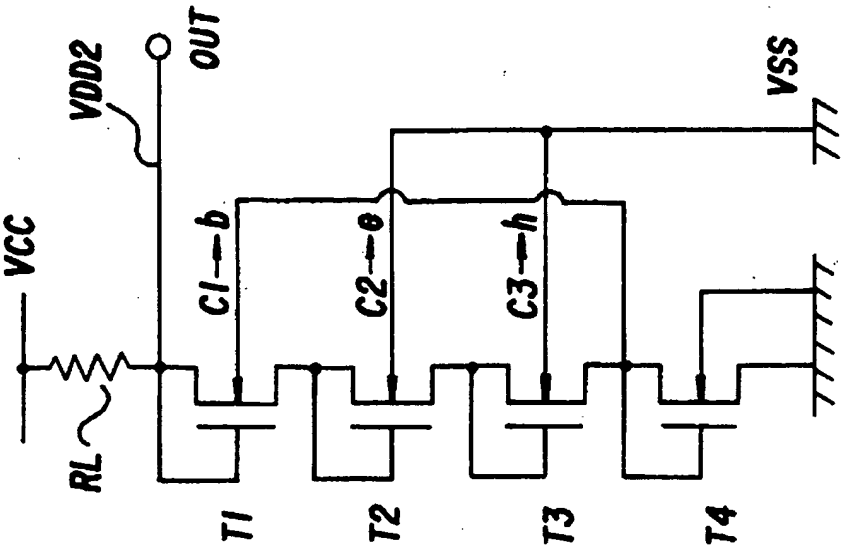

VDD2
OUT
VSS
VCC
C1—b
C2—e
C3—h
RL
T1
T2
T3
T4

FIG. 7A

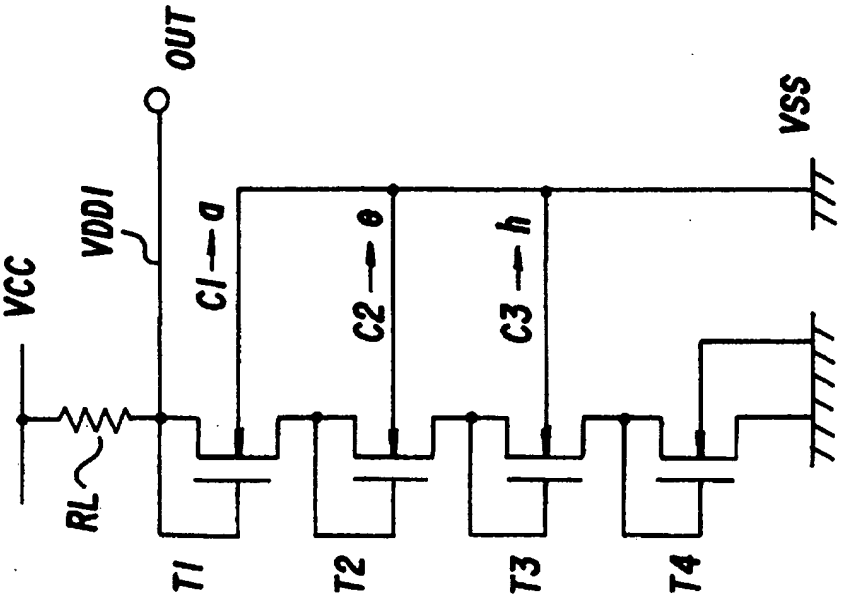

OUT
VSS
VDD1
VCC
C1—a
C2—e
C3—h
RL
T1
T2
T3
T4

FIG. 7D

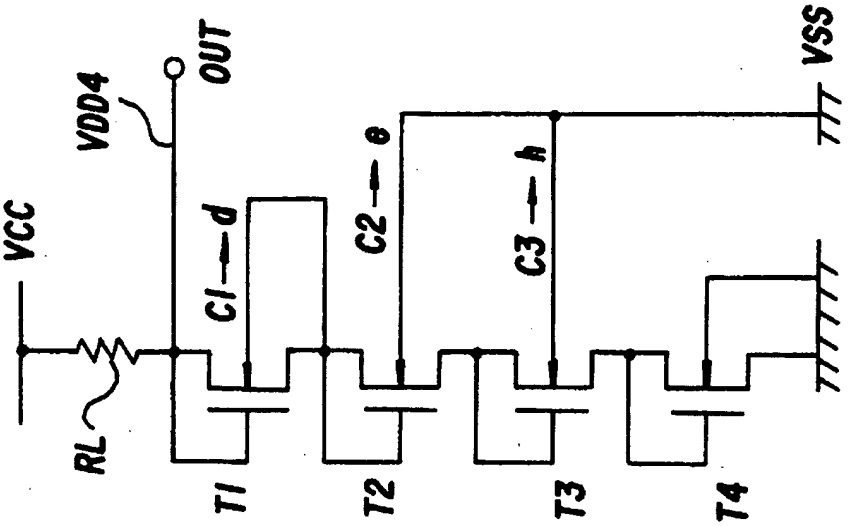

VCC
VDD4
OUT
VSS
C1—d
C2—e
C3—h
RL
T1
T2
T3
T4

FIG. 7C

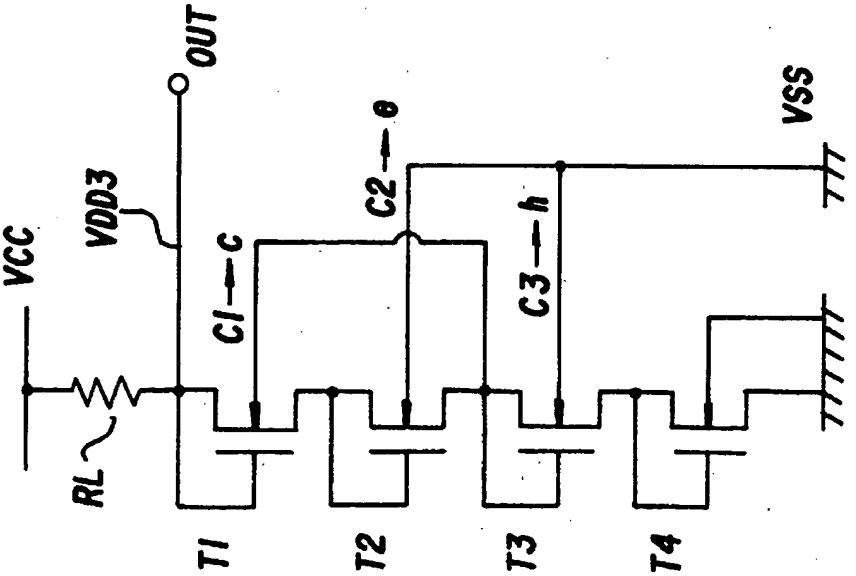

VCC
VDD3
OUT
VSS
C1—c
C2—e
C3—h
RL
T1
T2
T3
T4

FIG. 7F

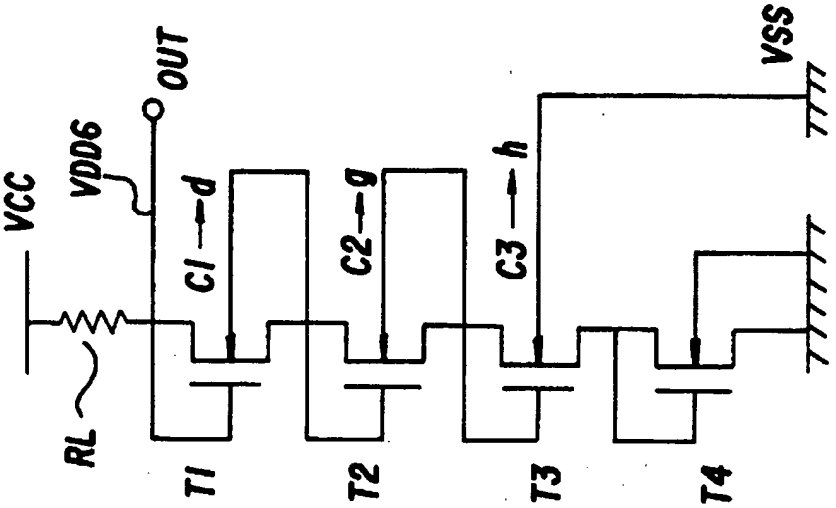

VCC
VDD6
OUT
C1—d
C2—g
C3—h
VSS
RL
T1
T2
T3
T4

FIG. 7E

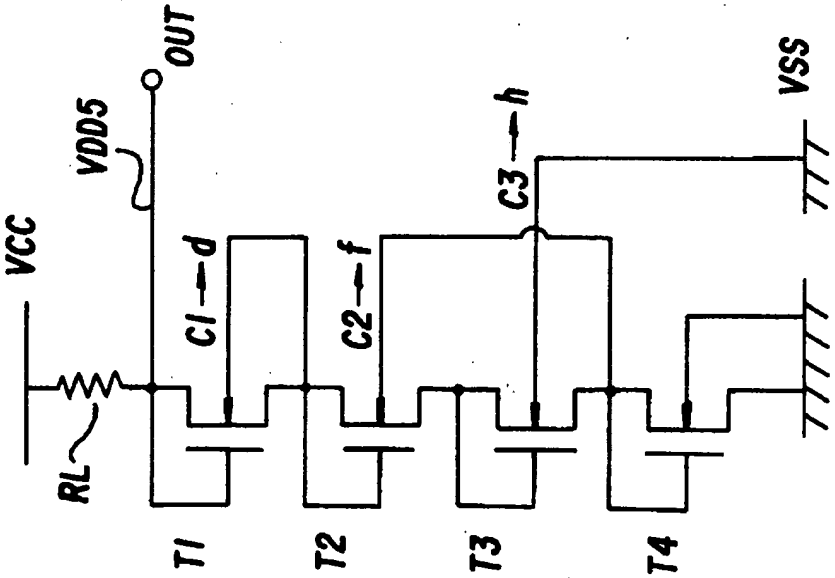

VCC
VDD5
OUT
C1—d
C2—f
C3—h
VSS
RL
T1
T2
T3
T4

FIG.8B

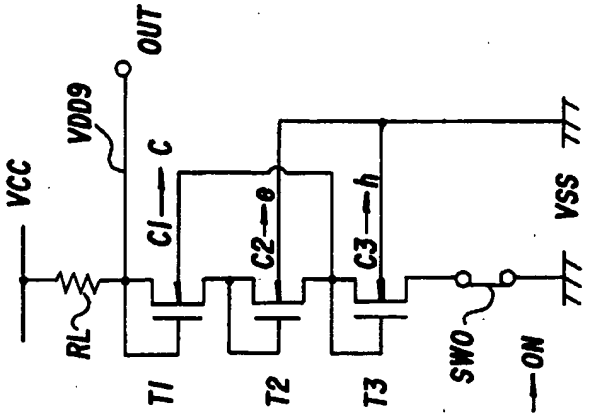


FIG.8A

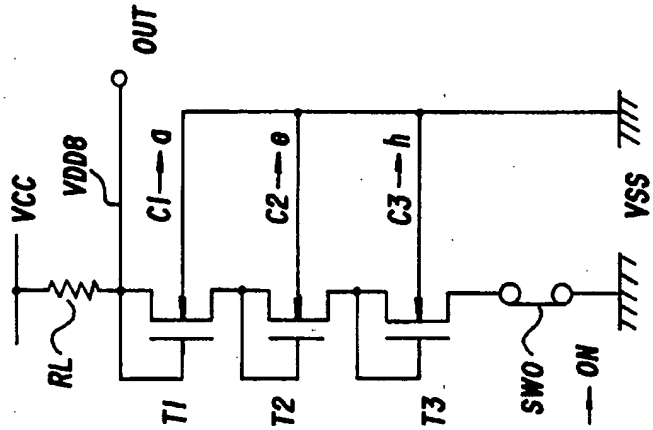


FIG.7G

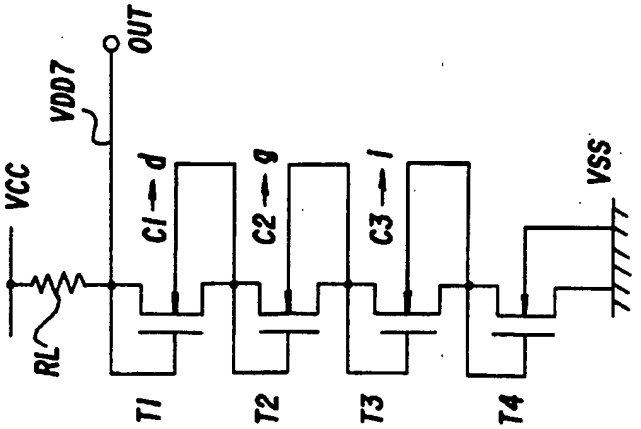


FIG.8D

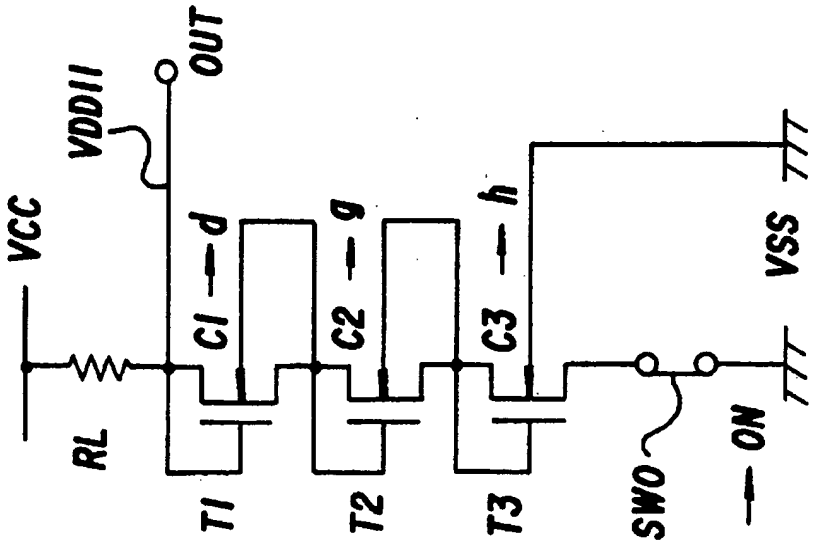

VCC
VDD11
OUT
C1 — d
C2 — g
C3 — h
VSS
RL
T1
T2
T3
SWO
— ON

FIG.8C

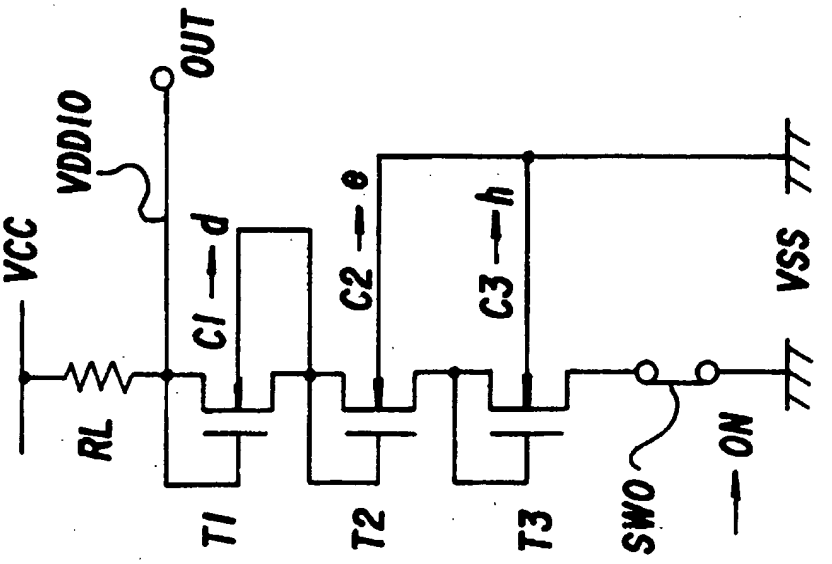
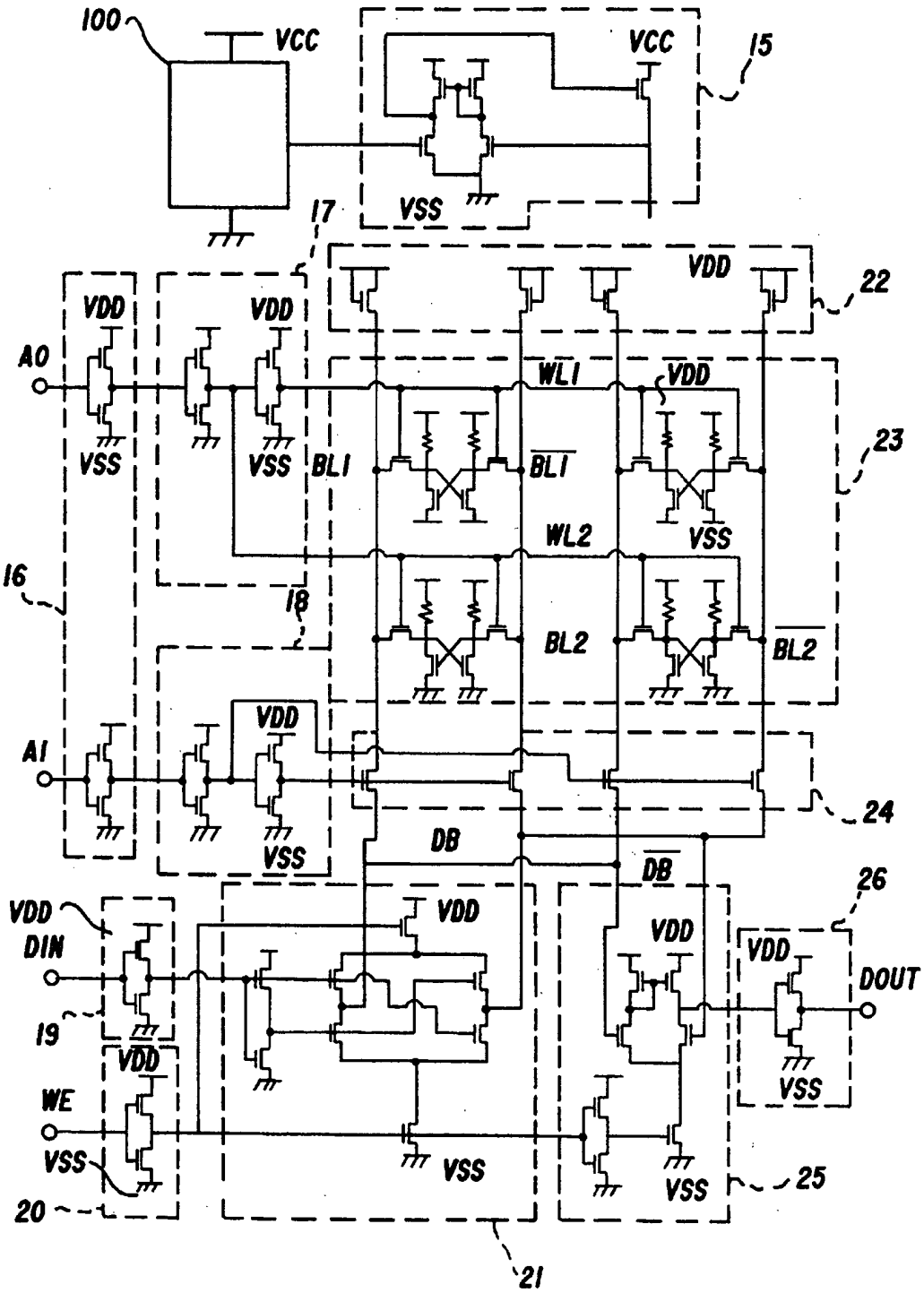

VCC
VDD10
OUT
C1 — d
C2 — e
C3 — h
VSS
RL
T1
T2
T3
SWO
— ON

FIG.9


100
VCC
VCC
15
VSS
17
VDD
22
VDD
VDD
A0
WL1
VDD
VSS
VSS
BL1
BL1
23
WL2
VSS
16
18
BL2
BL2
VDD
A1
24
VSS
DB
DB
26
VDD
VDD
VDD
VDD
DIN
DOUT
19
VDD
VSS
WE
VSS
VSS
VSS
25
20
21

OUTPUT CIRCUIT FOR PROVIDING A FINALLY ADJUSTABLE VOLTAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a constant-voltage generator circuit and semiconductor memory, and more particularly, to the improvements of a circuit for generating a fine-adjusted constant voltage and low-voltage-driven memory.

2. Description of the Related Art

Recently, pattern microminiaturization is making a rapid progress in large scale integrated circuit (hereinafter referred to as "LSI") devices because of the needs for the smaller size and higher capacity, and the higher speed of transistor operation. This, in turn, reduces the resisting voltage of MOS transistors. As for semiconductor memory for storing information, for example, designers strive to reduce its driving voltage.

In order to supply high precision constant voltages to the low-voltage-driven semiconductor memory, designers usually use constant voltage generator circuits using a band gap or constant voltage generator circuits using the threshold voltage of field effect transistors.

However, adjusting steps of the constant voltage are limited to the selection ranges which depend on the thresholds of diode-configured transistors of a constant voltage circuit. Accordingly, the voltage adjustment fineness may become "rough" and a fine adjustment of the power supply voltage may need to be done for each load circuit because the thresholds vary with unevenness in transistor manufacturing.

Here, related arts of the invention will be explained. For example, as shown in FIG. 1 a first constant voltage generator circuit supplying a constant voltage V_{DD} to SRAM (static random access memory) comprises a transistor selection circuit 1, a load resistor RL1, and four transistors T11–T41. Note that the circuit is arranged in a manner where the back-gates BG1–BG4 of the four transistor T11–T41 are biased with a common voltage.

Specifically, the four transistors T11–T41 are composed of n-type field effect transistors, each of which is diode-configured. The four transistors T11–T41 are serially connected with the drain of transistor T11 connected to one end of a load resistor RL1 and connected to an output OUT. The other end of the load resistor RL1 is connected to the power source line V_{CC} and the source of the transistor T41 is connected to the ground line V_{SS}. The back-gates BG1–BG4 of the four transistors T11–T41 are connected together to the ground line V_{SS}. And, each of source-drain connection points of the transistors T11–T41 is connected to a transistor selection circuit 1.

The transistor selection circuit 1 comprises three switching devices TS1–TS3, the connections of which are controlled on the basis of external control signal S. The switching device TS1 is connected between the source-drain connection points of the transistors T11 and T21 and the transistors T21 and T31. The switching device TS2 is connected between the source-drain connection points of the transistors T21 and T31 and the transistors T31 and T41. The switching device TS3 is connected between the source-drain connection point of the transistors T31 and T41 and the ground line V_{SS}.

The above-described constant voltage generator circuit functions as follows: when switching devices TS1–TS3 are selected and connected on the basis of an external control signal S, diode-configured transistors T21–T41 are selected; this causes the voltage between the power source line Vcc and the ground line V_{SS} to be divided by the load resistor RL1 and the serially connected transistors T11–T41, where each resistance of the transistors T11–T41 in the conducting (or ON) state exhibits a value which depends on the substantially constant threshold VTH; and a constant voltage VDD is generated at the output OUT.

Further, a second constant voltage generator circuit according to related arts of the present invention comprises a transistor selection circuit 2, a load resistor RL2, and four transistors T12–T42 as shown in FIG. 2. In this circuit, the back-gates of the four transistors T12–T42 are biased with different voltages.

As in the first constant voltage generator circuit, the four transistors T12–T42, each of which is in a diode configuration, are connected in a series. The drain of transistor T12 is connected to one end of the load resistor RL2 and the output OUT. The other end of the load resistor RL2 is connected to the power source line V_{CC} and the source of the transistor T42 is connected to the ground line VSS.

The back-gate BG1 of the transistor T12 is connected to the source-drain connection point of the transistors T12 and T22, the back-gate BG2 of the transistor T22 is connected to the source-drain connection point of the transistors T22 and T32, the back-gate BG3 of the transistor T32 is connected to the source-drain connection point of the transistors T32 and T42. And the back-gate BG4 of the transistor T42 is connected to the ground line V_{SS}.

The transistor selection circuit 2 comprises three switching devices TS1–TS3 and their connections are controlled on the basis of an external control signal S. The switching device TS1 is connected between the source-drain connection points of the transistors T12 and T22 and the transistors T22 and T32. The switching device TS2 is connected between the source-drain connection points of the transistors T22 and T32 and the transistors T32 and T42. The switching device TS3 is connected between the source-drain connection point of the transistors T32 and T42 and the ground line V_{SS}.

The constant voltage generator circuit functions as follows: when switching devices TS1–TS3 are selected and connected on the basis of an external control signal S, diode-configured transistors T21–T41 are selected; this causes the voltage between the power source line V_{CC} and the ground line V_{SS} to be divided by the load resistor RL2 and the transistors T12–T42, where each resistance of the transistors T11–T41 in the conducting state exhibits a value which depends on a different threshold VTH; and a constant voltage VDD is generated at the output OUT.

SUMMARY OF THE INVENTION

The object of the present invention is to provide an extremely fine voltage adjustment by forming a simple circuit where thresholds of transistors are made use of and by devising a new way of biasing back-gates. In other words, it is to generate constant voltages in fine steps by dividing the power source voltage by the resistance in the conducting state which depends on the thresholds of n transistors and a load resistor connected to the power source line.

The further object of the invention is to enhance the reliability of a circuit where an inventive constant voltage generator circuit is applied by providing a ROM fuse circuit, programming the fuse devices to generate an external con-

trol signal, and vary finely adjusting the bias voltages of back-gates in the constant voltage generator circuit according to the external control signal.

That is, a preferred embodiment of the constant voltage generator circuit according to the present invention, comprising adjusting means for making fine adjustment of each back-gate voltage of transistors on the basis of external control signals, and a transistor circuit for outputting a constant voltage adjusted on the basis of the back-gate voltage.

A constant voltage generator circuit comprises adjusting means for making fine adjustment of each back-gate voltage of transistors on the basis of external control signals; and a transistor circuit for outputting a constant voltage adjusted on the basis of the back-gate voltages, the transistor circuit includes a plurality of N transistors with their respective gates and drains connected together, and a load element for dividing the power source voltage with a plurality of N transistors.

A constant voltage generator circuit comprises a transistor circuit for outputting a constant voltage adjusted on the basis of back-gate voltages, the transistor circuit includes a plurality of N transistors with their respective gates and drains connected together, and a load element for dividing the power source voltage with a plurality of N transistors; a ROM fuse circuit for generating the external control signals; and adjusting means for making fine adjustment of each back-gate voltage of a plurality of transistors on the basis of the external control signals.

Adjusting means comprises a plurality of N−1 switching circuits for supplying bias voltages individually to the back-gate of the first through (N−1)th transistors in the transistor circuit on the basis of the external control signal, and a switching element for stopping the operation of the Nth transistor in the transistor circuit on the basis of the external control signal.

The first switching circuit of the adjusting means, on the basis of the external control signal, is for biasing the back-gate of the first transistor in the transistor circuit with an selected one out of the source voltage between the first and second serially-connected transistors, the source voltage between the second and third transistors, . . . , the source voltage between the (N−1)th and Nth transistors, and the power source voltage of the lower side.

The second switching circuit of the adjusting means, on the basis of the external control signal, is for biasing the back-gate of the second transistor in the transistor circuit with an selected one out of the source voltage between the second and third serially-connected transistors, the source voltage between the third and forth transistors, . . . , the source voltage between the (N−1)th and (n)th transistors, and the power source voltage of the lower side.

The (N−1)th switching circuit of the adjusting means, on the basis of the external control signal, for biasing the back-gate of the (N−1)th transistor in the transistor circuit with an selected one out of the source voltage between the (N−1)th and Nth serially-connected transistors, and the power source voltage of the lower side.

External control signals are generated by programming the fuse elements of the ROM fuse circuit. The transistor circuit is formed of n-type field effect transistors.

A semiconductor memory comprises memory means for storing information, and constant voltage generating means for supplying voltage to memory means. The constant voltage generating means includes adjusting means for making fine adjustment of each back-gate voltage of a plurality of transistor on the basis of external control signals, and a transistor circuit for outputting the constant voltage adjusted on the basis of the back-gate voltages.

The transistor circuit includes a plurality of N transistors with their respective gates and drains connected together,and a load element for dividing the power source voltage with a plurality of N transistors. The constant voltage generating means further comprises a ROM fuse circuit for generating the external control signals.

Employing such circuit configurations yields a constant voltage generating circuit permitting voltage adjustment by a fine step and low-voltage-driven reliable semiconductor memory to which the constant voltage generating circuit is applied.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram showing the arrangement of a transistor-selecting-type constant voltage generator circuit according art which is related to the present invention;

FIG. **2** is a diagram showing the arrangement of another transistor-selecting-type constant voltage generator circuit according art which is related to the invention;

FIG. **3** is a diagram showing the arrangement of a fundamental constant voltage generator circuit according to the invention;

FIG. **4** is a diagram showing the fundamental arrangement of semiconductor memory to which the constant voltage generator circuit shown in FIG. **3** is applied;

FIG. **5** is a diagram showing the arrangement of a constant voltage generator circuit according to a preferred embodiment of the present invention;

FIG. **6** shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **5**;

FIG. **7**A through **7**G each shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (SW0=OFF);

FIG. **7**A shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→a, C2→e, and C3→h);

FIG. **7**B shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→b, C2→e, and C3→h);

FIG. **7**C shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→c, C2→e, and C3→h);

FIG. **7**D shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→d, C2→e, and C3→h);

FIG. **7**E shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→d, C2→f, and C3→h);

FIG. **7**F shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→d, C2→g, and C3→h);

FIG. **7**G shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→d, C2→g, and C3→i);

FIG. **8**A through **8**D each shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (SW0=ON);

FIG. **8**A shows an equivalent circuit of the constant voltage generator circuit shown in FIG. **6** when programming (C1→a, C2→e, and C3→h);

FIG. 8B shows an equivalent circuit of the constant voltage generator circuit shown in FIG. 6 when programming (C1→c, C2→e, and C3→h);

FIG. 8C shows an equivalent circuit of the constant voltage generator circuit shown in FIG. 6 when programming (C1→d, C2→e, and C3→h);

FIG. 8D shows an equivalent circuit of the constant voltage generator circuit shown in FIG. 6 when programming (C1→d, C2→g, and C3→h); and

FIG. 9 is a diagram showing the arrangement of a static random access memory (SRAM) in which a constant voltage generator circuit according to an embodiment of the invention is utilized.

DETAILED DESCRIPTION

According to a first constant voltage generator circuit of related arts of the invention, as shown in FIG. 1, a transistor selection circuit 1 is provided, and some of the four transistors T11–T41 are selected on the basis of the external control signal S. Thus, through the selection of the transistors T11–T41, it is possible to obtain a constant voltage V_{DD} which is the allotted portion of the voltage between the power source line V_{CC} and the ground line V_{SS} divided by the ON-state (or conducting-state) resistances which depend on a substantially constant threshold VTH and the load resistor RL1.

Also, according to a second constant voltage generator circuit of related arts of the invention, a transistor selection circuit 2 is provided, and some of the four transistors T12–T42 are selected on the basis of the external control signal S. Thus, through the selection of the transistors T12–T42, it is possible to obtain a constant voltage V_{DD} which is the allotted portion of the voltage between the power source line V_{CC} and the ground line V_{SS} divided by the ON-state resistances which depend on different thresholds VTH and the load resistor RL2.

However, what is true to both first and second constant voltage generator circuit is that the adjusting steps for the constant voltage are limited within selection ranges which depend on the thresholds VTH of the diode-configured transistors T11–T41 or T12–T42, which causes its voltage adjusting fineness to be "rough". Additionally, when thresholds VTH varies owing to unevenness in manufacturing of transistors T11–T41 or T12–T42, a fine adjustment of the constant voltage V_{DD} becomes necessary for every load circuit.

This prevents a high-precision constant voltage V_{DD} from being supplied to minutely processed low-voltage-driven SRAM and the like. Thus, unevenness in manufacturing may result in lack of stability of circuit operation or degradation of reliability of its application system.

On the other hand, a fundamental constant voltage generator circuit of the invention, as shown in FIG. 3, is provided with a load element RL, a bias variable means 11, and a plurality of n field effect transistors Tn (n=1,2, . . . ,n). The n transistors, each of which is in a diode configuration, are connected in a series. One end (of T1) of the serially connected transistors is connected to one end of the load element RL and the output OUT. The other end of the load element RL is connected to the first power source line V_{CC} and the other end (of Tn) of the serially connected transistors is connected to the second power source line V_{SS}. The back-gates BGn (n=1,2, . . . ,n) of the n transistors Tn are connected to the bias variable means 11, the outputs of which are controlled on the basis of the external control signal S.

Specifically, in the fundamental constant voltage generator circuit of the invention, the bias variable means 11 comprises a switching element 11A and n−1 selection switching circuits SWk (k=1,2, . . . ,n−1). The back-gate BGk of a transistor Tk is connected individually to the common contact Ck of the respective selection switching circuit Swk. The source-drain connection points between the serially connected transistors Tn are connected to contacts a, b, c, d, ... The back-gate Bgn of the transistor Tn connected to the second power source line V_{SS} is connected to the second power source line V_{SS}. The switching element 11A is connected in parallel to the transistor Tn connected to the second power source line V_{SS}.

Further, in the fundamental constant voltage generator circuit of the invention, to the back-gates Bgn (n=1,2, . . . ,n) of the n transistors Tn, there are supplied voltages of source-drain connection points between serially connected transistors Tn or the voltage of the second power source line V_{SS}.

Further, in the fundamental constant voltage generator circuit of the invention, output control for the bias variable means 11 is achieved by providing a ROM fuse circuit 14 for generating the external control signal S and programming the fuse elements FU in the ROM fuse circuit 14.

Still further, as shown in FIG. 4, the fundamental semiconductor memory of the invention is provided with a memory means 12 for storing information and a power supplying means 13 for supplying a power source to the memory means 12. The inventive constant voltage generator circuit 100 is connected to the power supplying means 13.

Operation of the fundamental constant voltage generator circuit of the invention will be described below. For example, as shown in FIG. 3, the fuse elements FU in a ROM fuse circuit 14 is programmed to generate the external control signal S, on the basis of which the bias variable means 11 has its output finely controlled. That is, connecting the common contacts Ck of the selection switching circuits Swk and contacts a, b, c, d, . . . selectively on the basis of the external control signal S causes the back-gate Bgn of the n transistors T1–Tn to be biased selectively with voltages supplied to the contact a, b, c, d, . . . —for example, voltages of source-drain connection points between transistors Tn and the voltage of the second power source line V_{SS}.

Accordingly, there is obtained a constant voltage V_{DD} to which the ON-state resistance dependant on the threshold of Tn of the n transistors T1–Tn and the load resistor RL connected to the first power source line V_{CC} proportionally allocate the voltage between the power source lines V_{CC} and VSS. At this time, the threshold VTH of the n transistors T1–Tn varies in more fine steps as compared with the related art of the invention. This is because the voltage impressed on each back-gate Bgn of the transistors T1–Tn is biased with a selected strength of voltage.

Therefore, even when thresholds VTH of the transistors T1–Tn varies owing to unevenness in manufacturing, a constant voltage V_{DD} adjusted by fine steps is supplied for each load circuit which requires a strict precision of the voltage. That is, the adjustment of the constant voltage is achieved with high precision.

Further, the operation of a fundamental semiconductor memory of the invention will be described below. For example, as shown in FIG. 4, the fuse elements FU of the ROM fuse circuit 14 are programmed to generate the said external control signal S, on the basis of which the bias

voltages of the back-gates of the constant voltage generator circuit is minutely adjusted. Therefore, it is possible to supply constant voltages V_{DDi} (i=1,2, . . . ,n), with precision, which is suitable for minutely-processed low-voltage-driven SRAM which has an extremely limited allowable of the operation voltage and the like.

Therefore, the optimum constant voltage V_{DDi} is supplied for manufacture unevenness of transistors constituting the memory means **12**. This contributes greatly to the manufacturing of semiconductor memory of high reliability such as low-voltage-driven SRAM's.

Next, we discuss illustrative embodiments of the present invention referring to the drawings.

(1) Constant Voltage Generator Circuit

For example, as shown in FIG. **5**, a constant voltage generator circuit for supplying a constant voltage to a load circuit which requires a strict precision of the power source voltage comprises transistors T1–T4, a load resistor RL, a switching element **SW0**, selection switching circuits SW1–SW3, inverter INV1–INV4, and a ROM fuse circuit **14**.

That is, the transistors T1–T4 are one example set of n transistors T1–Tn, indicating the case of n=4. The four transistors T1–T4 are composed of n-type field effect transistors. Each of the transistors T1–T4 has its gate connected to its drain (hereinafter, referred to as "is diode-configured"). Also, the four transistors T1–T4 are connected in a series (source-drain connection). One end of the transistor T1 and one end of the load resistor RL are connected together to the output OUT. And, the source and the back-gate of the transistor T4 are connected to the second power source line (hereinafter, referred to as "the ground line") V_{SS}.

The load resistor RL, which is an example of the load element RL, has its one end connected to the first power source line (hereinafter, simply referred to as "the power source line") V_{CC} of about 3V. As the load resistor RL, one or more transistor with less current-driving capability than the transistors T1–T4 are used.

The switching element **SW0** and selection switching circuit SW1–SW3 are an illustrative example of a bias variable means **11**, and the switching element SW0 is an example of the switching element **11A**. The selection switching circuits SW1–SW3 are one example of k pieces of selection switching circuits Swk, indicating the case of k=3.

The switching element **SW0** is composed of an n-type field effect transistor. The transistor TN4 has its source connected to the ground line V_{SS}, its drain connected to the source-drain connection of the transistors T3 and T4, and its gate connected to the ROM fuse circuit **14** via the inverter INV4.

The selection switching circuit SW1 is composed of 4 pieces of p-type field effect transistors TP1–TP4. The sources of the transistors TP1–TP4 are connected together to the back-gate BG1 of the transistor T1. The drain of the transistor TP1 is connected to the source-drain connection point of the transistors T1 and T2, and its gate is connected to the ROM fuse circuit **14**. The drain of the transistor TP2 is connected to the source-drain connection point of the transistors T2 and T3, and its gate is connected to the ROM fuse circuit **14**. The drain of the transistor TP3 is connected to the source-drain connection point of the transistors T3 and T4, and its gate is connected to the ROM fuse circuit **14**. The drain of the transistor TP4 is connected to the ground line V_{SS} and its gate is connected to the ROM fuse circuit **14**.

The selection switching circuit SW2 is composed of 3 pieces of p-type field effect transistors TP5–TP7. The sources of the transistors TP5–TP7 are connected together to the back-gate BG2 of the transistor T2. The drain of the transistor TP5 is connected to the source-drain connection point of the transistors T2 and T3, and its gate is connected to the ROM fuse circuit **14**. The drain of the transistor TP6 is connected to the source-drain connection point of the transistors T3 and T4, and its gate is connected to the ROM fuse circuit **14**. The drain of the transistor TP7 is connected to the ground line V_{SS} and its gate is connected to the ROM fuse circuit **14** via the inverter INV2.

The selection switching circuit SW3 is composed of 2 pieces of n-type field effect transistors TN1 and TN2. The drains of the transistors TN1 and TN2 are connected together to the back-gate BG3 of the transistor T3. The source of the transistor TN1 is connected to the source-drain connection point of the transistors T3 and T4, and its gate is connected to the ROM fuse circuit **14** via the inverter INV3. The source of the transistor TN2 is connected to the ground line V_{SS} and its gate is connected to the ROM fuse circuit **14**.

Specifically, one circuit worth of the ROM fuse circuit **14** for generating the external control signal S is composed of an inverter INV, a resistor R and a fuse FU. The resistor R and the fuse element FU is connected in a series between the power source line V_{CC} and the ground line V_{SS} and an inverter INV is connected to the serial connection point. The output of the inverter INV plays a role of the external control signal Si (i=1, . . . ,10) and is supplied to the switching element SW0 and the selection switching circuit SW1–SW3. According to the external control signals S1–S10, the bias voltages are controlled.

FIG. **6** shows an equivalent circuit of a constant voltage generator circuit according to an illustrative embodiment of the invention. As shown in FIG. **6**, the selection switching circuit SW1 of the constant voltage generator circuit is replaced by a common contact C1 and contacts "a", "b", "c" and "d".

That is, the common contact C1 is a source-connection point of the transistors TP1–TP4 and is connected to the back-gate BG1 of the transistor T1. The contact "a" is the drain-connection point of the transistor TP4 and is connected to the ground line V_{SS}. The contact "b" is the drain-connection point of the transistor TP3 and is connected to the source-drain connection point of the transistor T3 and T4. The contact "c" is the drain-connection point of the transistor TP2 and is connected to the source-drain connection point of the transistor T2 and T3. The contact "d" is the drain-connection point of the transistor TP1 and is connected to the source-drain connection point of the transistor T1 and T2.

Also, the selection switching circuit SW2 is replaced by a common contact C2 and contacts "e", "f" and "g". That is, the common contact C2 is a source-connection point of the transistors TP5–TP7 and is connected to the back-gate BG2 of the transistor T2. The contact "e" is the drain-connection point of the transistor TP7 and is connected to the ground line V_{SS}. The contact "f" is the drain-connection point of the transistor TP6 and is connected to the source-drain connection point of the transistor T3 and T4. The contact "g" is the drain-connection point of the transistor TP5 and is connected to the source-drain connection point of the transistor T2 and T3.

Further, the selection switching circuit SW3 is replaced by a common contact C3 and contacts "h" and "i". That is, the common contact C3 is a drain-connection point of the transistors TN1–TN2 and is connected to the back-gate BG3 of the transistor T3. The contact "h" is the source-connection point of the transistor TN2 and is connected to the ground line V_{SS}. The contact "i" is the source-connection point of

the transistor TN1 and is connected to the source-drain connection point of the transistor T3 and T4.

Further, the switching element SW0 is a equivalent circuit of the transistor TN4 and is connected in parallel to the transistor T4. The equivalent circuits of the switching element and the selection switching circuit SW1–SW3 are formed as described above.

Next, referring to supplementary equivalent circuits, we discuss the operation at the time of programming of a constant voltage generator circuit according to the embodiment of the invention.

As an example, we discuss the case of programming the fuse elements of a ROM fuse circuit 14 for generating external control signals S1–S10, under the operating condition that the power source line V_{CC}=3V, each threshold VTH of the four transistors T1–T4 equals 0.4V when the back-gate voltage=0 and the VTH becomes higher by about 0.1V as the back-gate voltage drops by 0.4 V. In other words, VTH becomes lower by approximately 0.1V as the back-gate voltage increases by 0.4V. VTH increases by approximately 0.1V as gate voltage increases by 0.4V.

For example, as shown in FIG. 7A, in case of providing the constant voltage V_{DD1}=2.2V, the switching element SW0 is operated in the OFF state (hereinafter referred to as "OFF") and the common contact C1 of the selection switching circuit SW1 is connected to the contact "a" (hereinafter simply expressed as "C1→a"). Further, the common contact C2 of the selection switching circuit SW2 is connected to the contact "e" and the common contact C3 of the selection switching circuit SW3 is connected to the contact "h". To be concrete, the fuse elements FU of the ROM fuse circuit 14 are melted and disconnected to generate the external control signals S4, S7 and S9, which are supplied to each gate of the transistor TP4 in the selection switching circuit SW1, the transistor TP7 in the selection switching circuit SW2 and the transistor TN2 in the selection switching circuit SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD1}=2.2V, that is, the sum of 0.7V of the transistor T1 threshold VTH, 0.6V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH. The theoretical gate Voltage of transistor T4 is almost 0.4V, that of transistor T3 is almost 0.8V, that of transistor T2 is almost 1.2V, and that of transistor T1 is almost 1.6V. Therefore, VTH of transistor T3 increases by 0.1V and becomes 0.5V. Similarly, VTH of transistor T2 becomes 0.6V, and VTH of transistor T1 becomes 0.7V.

As shown in FIG. 7B, in case of providing the constant voltage V_{DD2}=2.1V, the connections are so made that SW0= "OFF", C1→b at SW1, C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S3, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP3 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively. The back gate of transistor T1 is connected to the source-drain connecting point of transistors T3 and T4, as shown in FIG. 7B. Therefore, the back-gate voltage of transistor T1 becomes 0.4V, thereby reducing VTH of transistor T1 by 0.1V. As a result, VTH of transistor T1 becomes 0.6V.

Thus, at the output OUT there is generated a constant voltage V_{DD2}=2.1 V, that is, the sum of 0.6V of the transistor T1 threshold VTH, 0.6V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Further, as shown in FIG. 7C, in case of providing the constant voltage V_{DD3}=2.0V, the connections are so made that SW0="OFF", C1→c at SW1, C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S2, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP2 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively. The back gate of transistor T1 is connected to the source-drain connecting point of transistors T2 and T3. Therefore, the back gate voltage of transistor T1 becomes 0.8V, thereby reducing VTH of transistor T1 by 0.2V. As a result, VTH of transistor T1 becomes 0.5V.

Thus, at the output OUT there is generated a constant voltage V_{DD3}=2.0 V, that is, the sum of 0.5V of the transistor T1 threshold VTH, 0.6V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Further, as shown in FIG. 7D, in case of providing the constant voltage V_{DD4}=1.9 V, the connections are so made that SW0="OFF", C1→d at SW1, C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S1, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP1 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD4}=1.9 V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.6V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Similarly, as shown in FIG. 7E, in case of providing the constant voltage V_{DD5}=1.8 V, the connections are so made that SW0="OFF", C1→d at SW1, C2→f at SW2 and C3→h at SW3. To be concrete, the external control signals S1, S6 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP1 in SW1, the transistor TP6 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD5}=1.8V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.5V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Further, as shown in FIG. 7F, in case of providing the constant voltage V_{DD6}=1.7 V, the connections are so made that SW0="OFF", C1→d at SW1, C2→G at SW2 and C3→h at SW3. To be concrete, the external control signals S1, S5 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP1 in SW1, the transistor TP5 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD6}=1.7 V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.4V of the transistor T2 threshold VTH, 0.5V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Further, as shown in FIG. 7G, in case of providing the constant voltage V_{DD7}=1.6V, the connections are so made that SW0="OFF", C1→d at SW1, C2→G at SW2 and C3→i at SW3. To be concrete, the external control signals S1, S5 and S8 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP1 in SW1, the transistor TP5 in SW2 and the transistor TN1 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD7}=1.6V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.4V of the transistor T2 threshold VTH, 0.4V of the transistor T3 threshold VTH and 0.4V of the transistor T4 threshold VTH.

Still further, as shown in FIG. 8A, in case of providing the constant voltage V_{DD8}=1.5V, the connections are so made that SW0="ON" C1→a at SW1 C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S4, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP4 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD8}=1.5V, that is, the sum of 0.6V of the transistor T1 threshold VTH, 0.5V of the transistor T2 threshold VTH and 0.4V of the transistor T3 threshold VTH.

Similarly, as shown in FIG. 8B, in case of providing the constant voltage V_{DD9}=1.4V, the connections are so made that SW0="ON", C1→c at SW1, C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S10, S2, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TN4 in SW0, the transistor TP2 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD9}=1.4V, that is, the sum of 0.5V of the transistor T1 threshold VTH, 0.5V of the transistor T2 threshold VTH and 0.4V of the transistor T3 threshold VTH.

Further, as shown in FIG. 8C, in case of providing the constant voltage V_{DD10}=1.3V, the connections are so made that SW0="ON" C1→d at SW1, C2→e at SW2 and C3→h at SW3. To be concrete, the external control signals S1, S7 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP4 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD10}=1.3V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.5V of the transistor T2 threshold VTH and 0.4V of the transistor T3 threshold VTH.

Further, as shown in FIG. 8D, in case of providing the constant voltage V_{DD11}=1.2V, the connections are so made that SW0="ON", C1→d at SW1, C2→g at SW2 and C3→h at SW3. To be concrete, the external control signals S1, S5 and S9 are generated in the ROM fuse circuit 14 and are supplied to each gate of the transistor TP4 in SW1, the transistor TP7 in SW2 and the transistor TN2 in SW3, respectively.

Thus, at the output OUT there is generated a constant voltage V_{DD12}=1.2V, that is, the sum of 0.4V of the transistor T1 threshold VTH, 0.4V of the transistor T2 threshold VTH and 0.4V of the transistor T3 threshold VTH.

In Table 1, the relations among the state of the switches, the thresholds VTH of each transistor, and constant (output) voltage are summarized.

TABLE 1

SWITCHES				TRANSISTOR				VOLTAGE	
SW	SW	SW	SW	VTH [V]				VDDi [V]	
1	2	3	0	T1	T2	T3	T4	T1 + T2 + T3 + T4	
a	e	h	OFF	0.7	0.6	0.5	0.4		2.2
b	↑	↑		0.6	↑	↑	↑		2.1
c	↑	↑		0.5	↑	↑	↑		2.0
d	↑	↑		0.4	↑	↑	↑		1.9
a	f	↑	↑	0.7	0.5	↑	↑	2.1	
b	↑	↑		0.6	↑	↑	↑	2.0	
c	↑	↑		0.5	↑	↑	↑	1.9	
d	↑	↑		0.4	↑	↑	↑		1.8

TABLE 1-continued

SWITCHES				TRANSISTOR				VOLTAGE	
SW	SW	SW	SW	VTH [V]				VDDi [V]	
1	2	3	0	T1	T2	T3	T4	T1 + T2 + T3 + T4	
a	g	↑	↑	0.7	0.4	↑	↑	2.0	
b	↑	↑		0.6	↑	↑	↑	1.9	
c	↑	↑		0.5	↑	↑	↑	1.8	
d	↑	↑		0.4	↑	↑	↑		1.7
a	e	i	↑	0.7	0.6	0.4	↑	2.1	
b	↑	↑		0.6	↑	↑	↑	2.0	
c	↑	↑		0.5	↑	↑	↑	1.9	
d	↑	↑		0.4	↑	↑	↑	1.8	
a	f	↑	↑	0.7	0.5	↑	↑	2.0	
b	↑	↑		0.6	↑	↑	↑	1.9	
c	↑	↑		0.5	↑	↑	↑	1.8	
d	↑	↑		0.4	↑	↑	↑	1.7	
a	g	↑	↑	0.7	0.4	↑	↑	1.9	
b	↑	↑		0.6	↑	↑	↑	1.8	
c	↑	↑		0.5	↑	↑	↑	1.7	
d	↑	↑		0.4	↑	↑	↑	1.6	
a	g	h	ON	0.6	0.5	0.4	—		1.5
c	↑	↑		0.5	↑	↑	—		1.4
d	↑	↑		0.4	↑	↑	—		1.3
a	g	h	↑	0.6	0.4	↑	—	1.4	
c	↑	↑		0.5	↑	↑	—	1.3	
d	↑	↑		0.4	↑	↑	—		1.2

NOTE
↑: SAME AS ABOVE

As shown in Table 1, though some values of the constant voltages V_{DDi} are repeated, the constant voltages V_{DDi} is adjusted by the step of 0.1V as described above. See the parts enclosed with meshes in Table 1.

In this way, in a constant voltage generator circuit according to an illustrative embodiment of the invention, as shown in FIG. 5, being provided with a load resistor RL, a switching element SW0, selection switching circuit SW1–SW3, four transistors T1–T4 and a ROM fuse circuit 14, the switching element SW0 and the selection switching circuit SW1–SW3 have their output controlled on the basis of the external control signals S1–S10.

For this reason, programming the ROM fuse circuit 14 enables very fine control of the outputs of the selection switching circuit SW1–SW3 as shown in Table 1. That is, by connecting the common contact C1 and the other contact a, b, c and d of the selection switching circuit SW1 selectively on the basis of the external control signals S1-S4, connecting the common contact C2 and the other contact e, f and g of the selection switching circuit SW2 selectively on the basis of the external control signals S5–S7,and connecting the common contact C3 and the other contact h and i of the selection switching circuit SW3 selectively on the basis of the external control signals S8 and S9. It is possible to bias the back-gates of the transistors T1–T4 with the voltages supplied to the contact "a" through "i" —for example, the voltages of the source-drain connection points between the transistors T1 and T2, T2 and T3, and T3 and T4, and the voltage of the power source line V_{SS}.

Therefore, it is possible to provide the constant voltage V_{DD1}=2.2V through V_{DD11}=1.2V to which the voltage between the power source line V_{CC} and the ground line V_{SS} is proportionally allotted by the ON-state resistance dependent on the thresholds of the transistors T1–T4 and the load resister RL connected to the power source line V_{CC}. In this operation, the thresholds of the transistors T1–T4 is changed through biasing by the step of 0.1 V, which is finer as compared with related arts. This is due to the voltages selectively supplied to the back-gates BG1–BG4 of the transistors T1–T4.

Accordingly, an optimal adjustment adapted for the load circuit is possible like constant voltages V_{DDi} shown in Table 1, even when the thresholds VTH varies because of manufacturing unevenness of the transistors T1–T4. Further, the adjustment of a constant voltage V_{DDi} is achieved with high precision.

(2) A Preferred Application Circuit of a Constant Voltage Generator Circuit

For example, as shown in FIG. **9**, a static random access memory (SRAM) for storing 4-bit data which is an example of semiconductor memory comprises a constant voltage generator circuit **100**, an internal power generator **15**, an address buffer **16**, a row decoder **17**, a column decoder **18**, an input buffer **19**, a WE buffer **20**, a write amplifier **21**, a bit line load **22**, a column transfer **23**, a cell array **24**, a sense amplifier **25**, and an output buffer **26** (hereinafter, referred to as "main parts **16** through **26**").

That is, the constant voltage generator circuit **100** and the internal power generator **15** form an example of a power supplying means **13**, and SRAM main parts **16** through **26** form a memory means **12**. The constant voltage generator circuit supplies constant voltage to SRAM main parts **16** through **26**. Here, the constant voltage generator circuit **100** is characterized in that it comprises a constant voltage generator circuit according to an embodiment of the invention.

The address buffer **16** inverts and supplies address **A0** and **A1** to the row decoder **17** and the column decoder **18**, respectively. The row decoder **17** selects one out of word lines **WL1** and **WL2** of the cell array **23**. The column decoder **18** generates signals for selecting among bit lines **BL1**, **B12**, $\overline{BL1}$ and $\overline{BL2}$ of the cell array **23**.

The input buffer **19** inverts and supplies a write data DIN to the write amplifier **21**. The WE buffer **20** inverts and supplies write/read enable signal $\overline{WE}$ to the write amplifier **21**. The write amplifier **21** amplifies a write data DIN according to the enable signal WE and write it to the cell array **23**. And, bit line load **22** supplies a constant voltage to the bit line BL1×2, BL2×2.

The column transfer **23** selects among bit lines **BL1**, **B12**, $\overline{BL1}$ and $\overline{BL2}$. The cell array **24** stores write data DIN. The sense amplifier **25** amplifies and outputs read data DB and $\overline{DB}$. The output buffer **26** inverts data DB and outputs them outside as output data DOUT.

The operation of the SRAM will be described below. For example in the write operation, when address **A0**, **A1** is specified for write data DIN, the address signal **A0** is inverted and supplied to the row decoder **17** and similarly the address **A1** is inverted and supplied to the column decoder **18**. Further, either word line **WL1** or **WL2** of the cell array **23** is selected in the row decoder **17**. The selection among bit lines **BL1**, **B12**, $\overline{BL1}$ and $\overline{BL2}$ of the cell array **23** is made by the column decoder **18** and the column transfer **24**. Then, write data DIN is inverted and supplied by the input buffer **19** to the write amplifier **21**, where it is amplified on the basis of the write/read enable signal WE to be written into the cell of the cell array **23** which is specified by the address **A0**, **A1**.

In read operation, when address **A0**, **A1** is specified for read data DB, the address signals **A0** and **A1** are inverted by the address buffer **16** to be supplied to the row decoder **17** and column decoder **18**, respectively. Also, the row decoder **17** selects either word line **WL1** or **WL2** of the cell array **23**, and the column decoder **18** makes selections among the bit lines **BL1**, **BL2**, $\overline{BL1}$ and $\overline{BL2}$. Then, read data DB, $\overline{DB}$ are amplified on the basis of the read/write enable signal WE by the sense amplifier **25** to be output outside from the output buffer **26** as an output data DOUT.

Thus, as shown in FIG. **8**, according to the SRAM which utilizes a constant voltage generator circuit according to an embodiment of the invention, there are provided a constant voltage generator circuit **100**, an internal power generator **15** and SRAM main parts **16** through **26**. And a constant voltage generator circuit according to an illustrative embodiment of the invention is applied to the said constant voltage generator circuit **100**.

Therefore, the output voltage of a constant voltage generator circuit is finely adjusted by means of bias control based on the external control signals **S1**–**S10** which are generated by programming the fuse elements FU of a ROM fuse circuit **14**. For this reason, an optimal constant voltage V_{DDi} is supplied with precision to each transistor circuit of minutely-processed low-voltage-driven SRAM, that is, an address buffer **16**, a row decoder **17**, a column decoder **18**, an input buffer **19**, a WE buffer **20**, a write amplifier **21**, a bit line load **22**, a column transfer **23**, a cell array **24**, a sense amplifier **25**, and an output buffer **26**.

This contributes greatly to an offer of reliable low-voltage-driven SRAM because an optimal power source voltage is provided for manufacturing unevenness of component transistors of SRAM main parts **16** through **26**.

What is claimed is:

1. An output voltage generator circuit, comprising:

a transistor circuit for outputting an output voltage, said transistor circuit comprising a plurality of transistors connected in series, wherein a source of a first transistor of said plurality of transistors is connected to a drain of a second, transistor of said plurality of transistors, and wherein each of said transistors is connected in a diode configuration; and

adjusting means connected to said transistor circuit, said adjusting means for separately adjusting a back-gate voltage of each transistor of said plurality of transistors, said adjusting means comprising switches connected to each of the plurality of transistors to selectively connect the backgate of said each transistor with a source of said each transistor or with a source of another transistor of said plurality of transistors which has a source voltage of at least one diode voltage threshold below the source of said each transistor, said back-gate voltages being controlled based upon control signals from an external source,

wherein said transistor circuit outputs an output voltage based upon adjustments by said adjusting means.

2. An output voltage generator circuit as recited in claim **1**, further comprising:

a load element for dividing a power source voltage with said plurality of transistors.

3. An output voltage generator circuit as recited in claim **1**, further comprising:

a ROM fuse circuit for generating said control signals.

4. An output voltage generator circuit according to claim **2** or **3**, wherein said adjusting means comprises:

(a) a plurality of switching circuits respectively connected to said plurality of transistors for supplying bias voltages individually to back-gates of each of the plurality of transistors in said transistor circuit, based upon the control signals; and

(b) a switching element for stopping an operation of a transistor in said transistor circuit based upon the control signals.

5. An output voltage generator circuit according to claim **2** or **3**, wherein a first switching circuit of said adjusting means, based upon the control signals, biases a back-gate of

the first transistor in said transistor circuit with one voltage selected from a group of voltages including

a source voltage between the first and second serially-connected transistors,

a source voltage between the second transistor and third transistor of said plurality of transistors,

a source voltage between the two adjacent transistors of said plurality of transistors, and

a power source voltage.

6. An output voltage generator circuit according to claim **2** or **3**, wherein a second switching circuit of said adjusting means, based upon the control signals, biases a back-gate of the second transistor in said transistor circuit with one voltage selected from a group of voltages including of

a source voltage between the second transistor and third transistor of said plurality of transistors,

a source voltage between the third transistor and a fourth transistor,

a source voltage between two adjacent transistors of said plurality of transistors, and

a power source voltage.

7. An output voltage generator circuit according to claim **2** or **3**, wherein a switching circuit of said adjusting means, based upon the control signals, biases a back-gate of one transistor of said transistor circuit with a voltage selected from a group of voltages including of

a source voltage between the one transistor and an adjacent transistor; and

a power source voltage.

8. An output voltage generator circuit according to claim **3**, wherein said control signal is generated by programming the fuse elements of said ROM fuse circuit.

9. An output voltage generator circuit according to claim **2** or **3**, wherein said transistor circuit comprising n-type field effect transistors.

10. A semiconductor memory comprising:

(a) memory means for storing information; and

(b) output voltage generating means for supplying voltage to said memory means, said output voltage generating means including

a transistor circuit for outputting said output voltage, said transistor circuit comprising a plurality of transistors connected in series, wherein a source of a first transistor of said plurality of transistors is connected to a drain of a second transistor of said plurality of transistors, and wherein each of said transistors is connected in a diode configuration; and

adjusting means connected to said transistor circuit, said adjusting meads for separately adjusting a back-gate voltage of each transistor of said plurality of transistors, said adjusting means comprising switches connected to each of the plurality of transistors to selectively connect the backgate of said each transistor with a source of said each transistor or with a source of another transistor of said plurality of transistors which has a source voltage of at least one diode voltage threshold below the source of said each transistor, said back-gate voltages being controlled based upon control signals from an external source,

wherein said transistor circuit outputs an output voltage based upon adjustments by said adjusting means.

11. A semiconductor memory according to claim **10**, wherein said transistor circuit further comprises

a load element for dividing a power source voltage with said plurality of transistors.

12. A semiconductor memory according to claim **10**, wherein said output voltage generating means further comprises a ROM fuse circuit for generating said control signals.

* * * * *

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United States Patent [19]

Javanifard et al.

[11] Patent Number: 5,483,486

[45] Date of Patent: Jan. 9, 1996

[54] **CHARGE PUMP CIRCUIT FOR PROVIDING MULTIPLE OUTPUT VOLTAGES FOR FLASH MEMORY**

[75] Inventors: **Jahanshir J. Javanifard**, Sacramento; **Marc E. Landgraf**, Folsom, both of Calif.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **326,654**

[22] Filed: **Oct. 19, 1994**

[51] **Int. Cl.**[6] **G11C 11/34**

[52] **U.S. Cl.** **365/185.17**; 365/189.09; 365/226; 327/536

[58] **Field of Search** 365/185, 189.09, 365/226, 230.06; 327/534, 536; 257/299

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1992 IEEE International Solid-State Circuits Conference, ISSCC 92 Session 9/Non-Volatile and Dynamic Rams/ Paper 9.3, "TP9.3: A 5V-Only 0.6 μm Flash EEPROM with Row Decoder Scheme in Triple-Well Structure", Masao Kuriyama, Shigeru Atsumi, Akira Umezawa, Hironori Banba, Ken-ichi Imamiya, Kiyomi Naruke, Seiji Yamada, Etsuishi Obi, Masamitsu Oshikiri, Tomoko Suzuki, Sumio Tanaka, pp. 152-153.

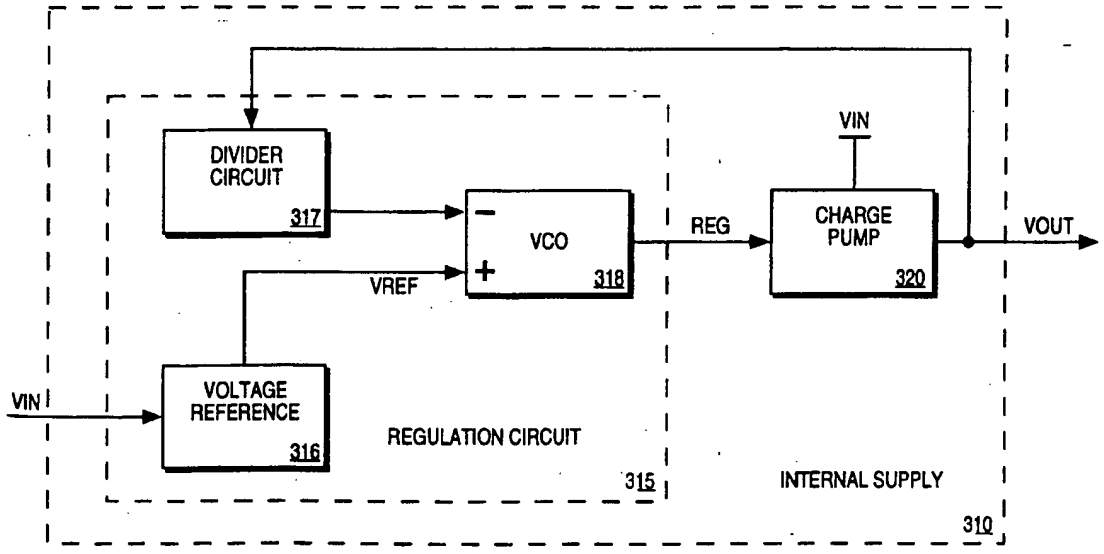
Primary Examiner—Joseph A. Popek

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A circuit for generating one of a plurality of output voltages. The circuit includes a first conductor coupled to a first supply voltage, a second conductor coupled to a second supply voltage, a charge pump having an input and an output, a multiplexor, a first regulation circuit, and a second regulation circuit. The first regulation circuit is coupled to the first input of the multiplexor and the output of the charge pump. The first regulation circuit is for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first output voltage when the first input of the multiplexor is coupled to the output of the multiplexor. The second regulation circuit is coupled to the second input of the multiplexor and the output of the charge pump. The second regulation circuit is for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second output voltage when the second input of the multiplexor is coupled to the output of the multiplexor. The multiplexing of the regulation circuitry results in a reduced number of components.

24 Claims, 24 Drawing Sheets



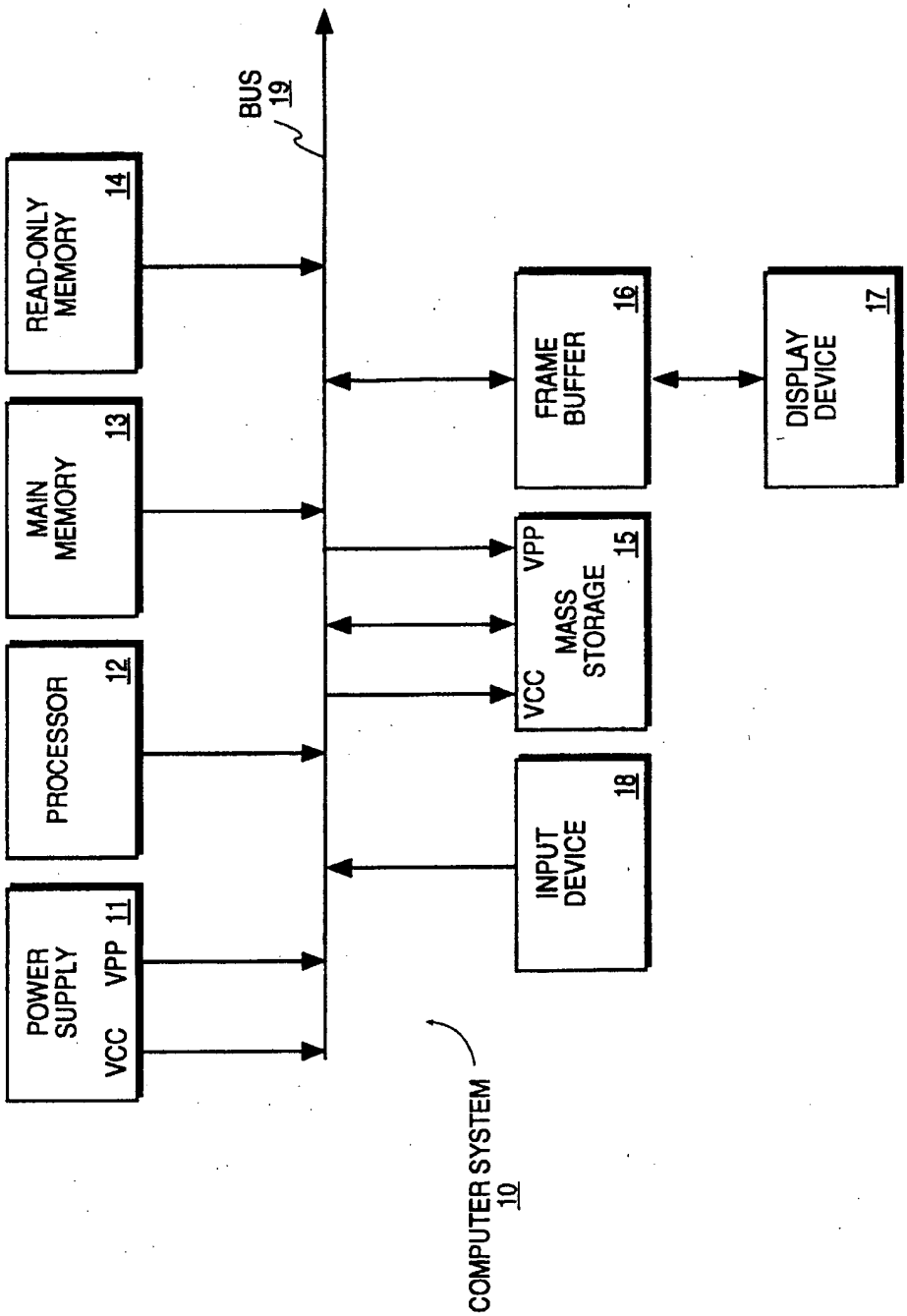

BUS
19
READ-ONLY MEMORY
14
MAIN MEMORY
13
PROCESSOR
12
POWER SUPPLY
11
VCC
VPP
FRAME BUFFER
16
DISPLAY DEVICE
17
MASS STORAGE
15
VPP
VCC
INPUT DEVICE
18
COMPUTER SYSTEM
10

FIG. 1

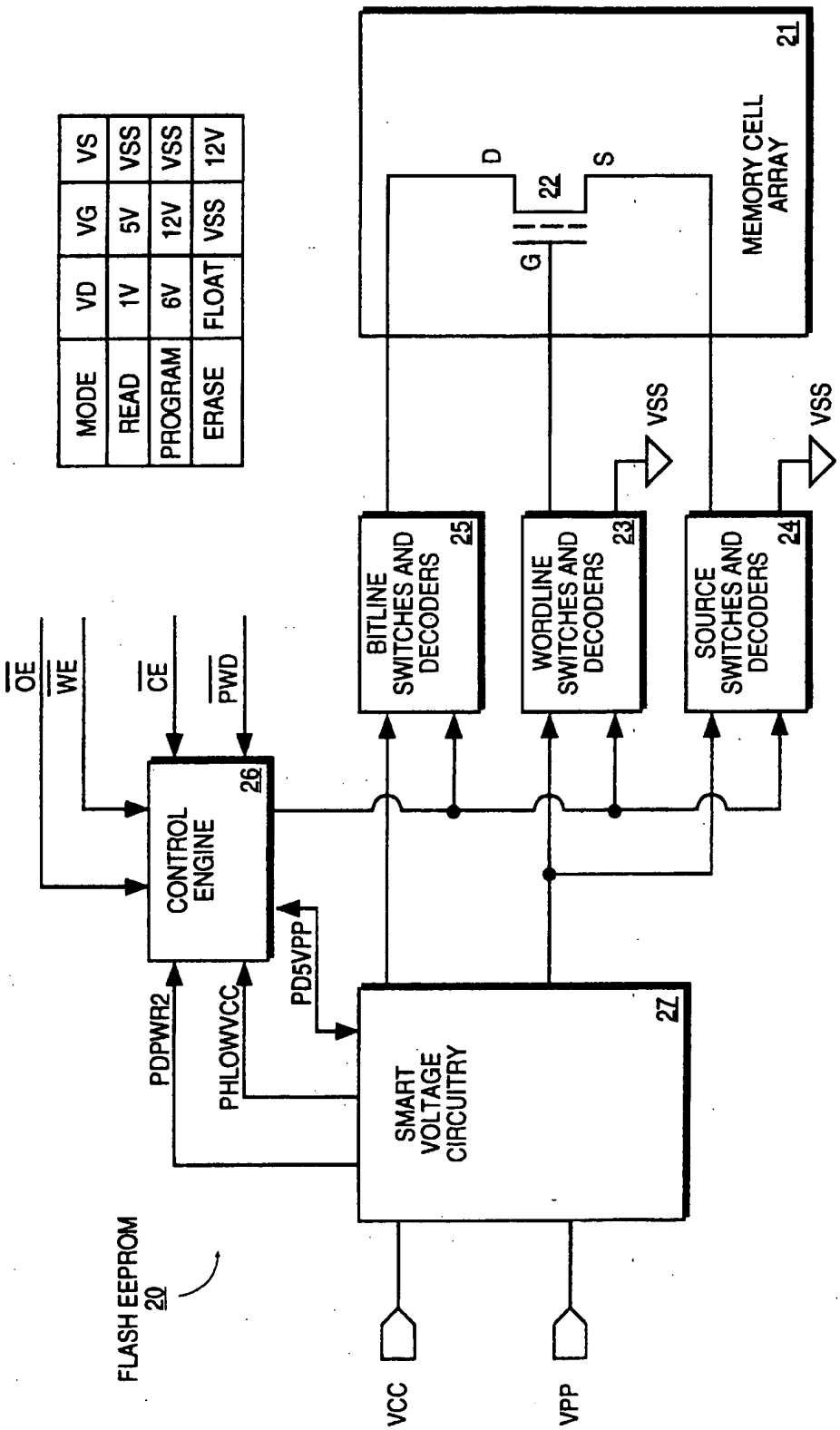

MODE
READ
PROGRAM
ERASE
VD
1V
6V
FLOAT
VG
5V
12V
VSS
VS
VSS
VSS
12V
MEMORY CELL ARRAY
21
D
S
G
22
BITLINE SWITCHES AND DECODERS
25
WORDLINE SWITCHES AND DECODERS
23
SOURCE SWITCHES AND DECODERS
24
VSS
VSS
OE
WE
CE
PWD
CONTROL ENGINE
26
PDPWR2
PHLOWVCC
PD5VPP
SMART VOLTAGE CIRCUITRY
27
FLASH EEPROM
20
VCC
VPP

FIG. 2

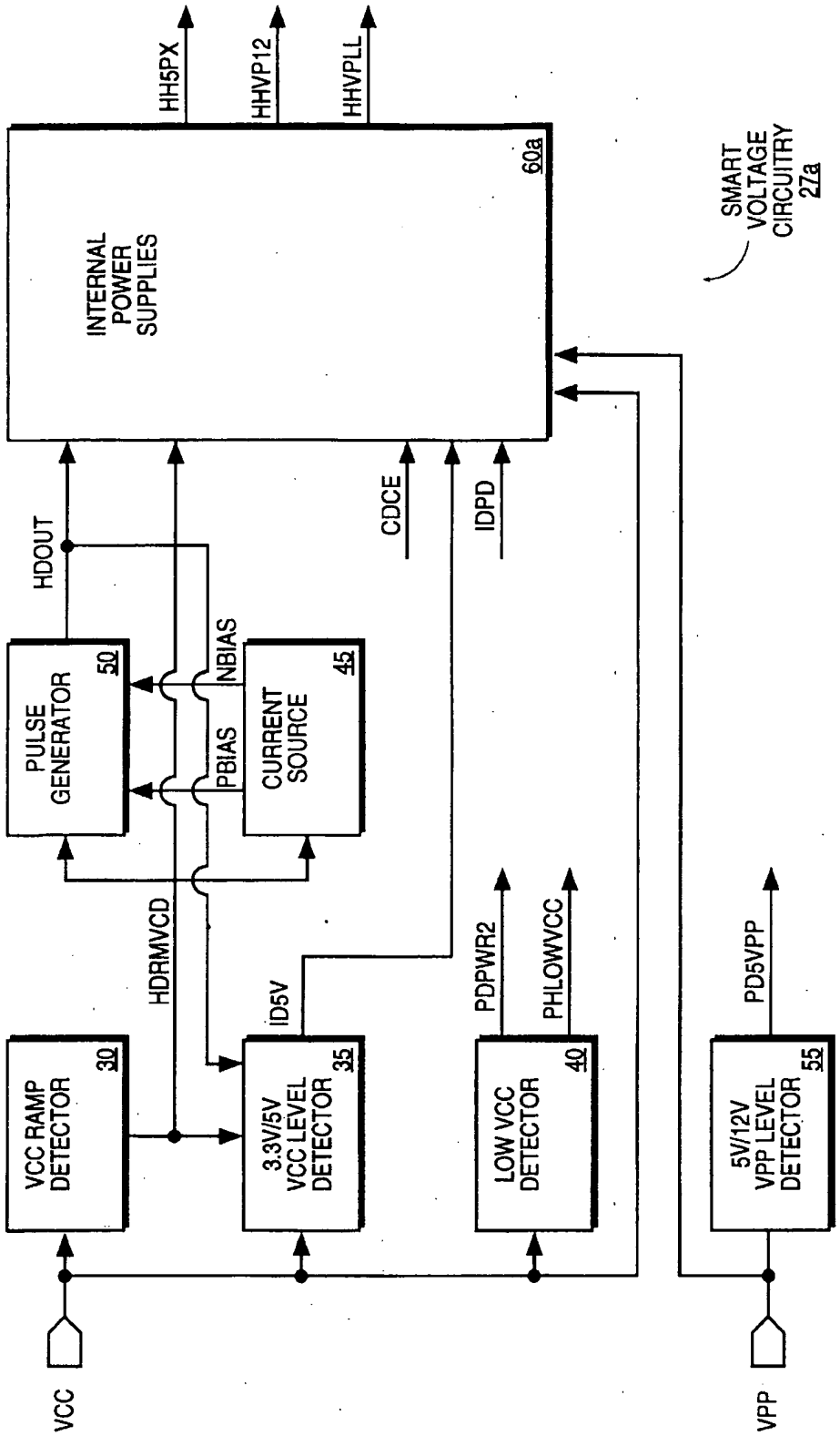

HH5PX
HHVP12
HHVPLL
INTERNAL POWER SUPPLIES
60a
SMART VOLTAGE CIRCUITRY 27a
CDCE
IDPD
HDOUT
PULSE GENERATOR
50
NBIAS
PBIAS
CURRENT SOURCE
45
HDRMVCD
ID5V
PDPWR2
PHLOWVCC
PD5VPP
VCC RAMP DETECTOR
30
3.3V/5V VCC LEVEL DETECTOR
35
LOW VCC DETECTOR
40
5V/12V VPP LEVEL DETECTOR
55
VCC
VPP

FIG. 3A

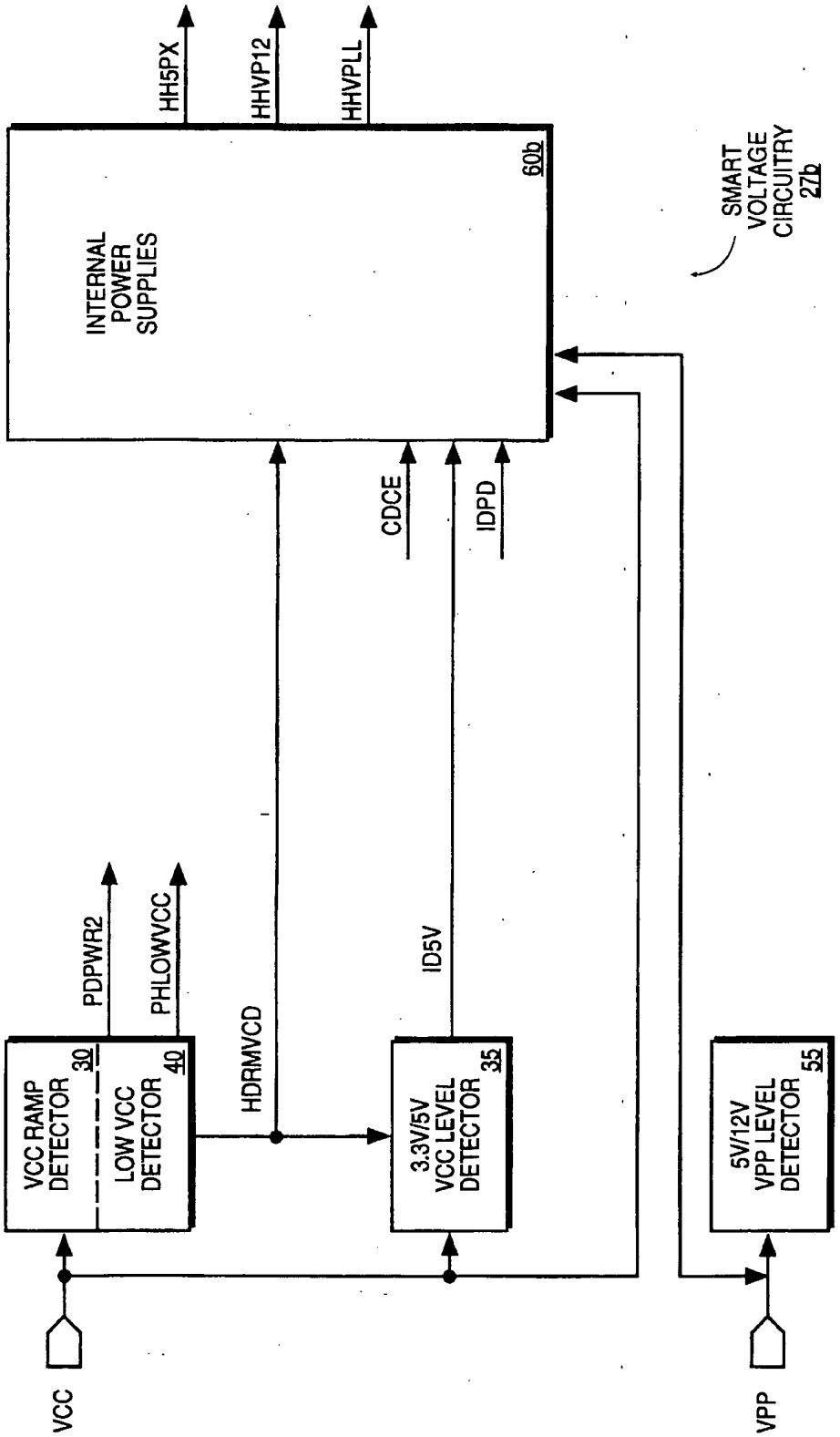

HH5PX
HHVP12
HHVPLL
INTERNAL POWER SUPPLIES
60b
SMART VOLTAGE CIRCUITRY 27b
CDCE
IDPD
PDPWR2
PHLOWVCC
HDRMVCD
ID5V
VCC RAMP DETECTOR 30
LOW VCC DETECTOR 40
3.3V/5V VCC LEVEL DETECTOR 35
5V/12V VPP LEVEL DETECTOR 55
VCC
VPP

FIG. 3B

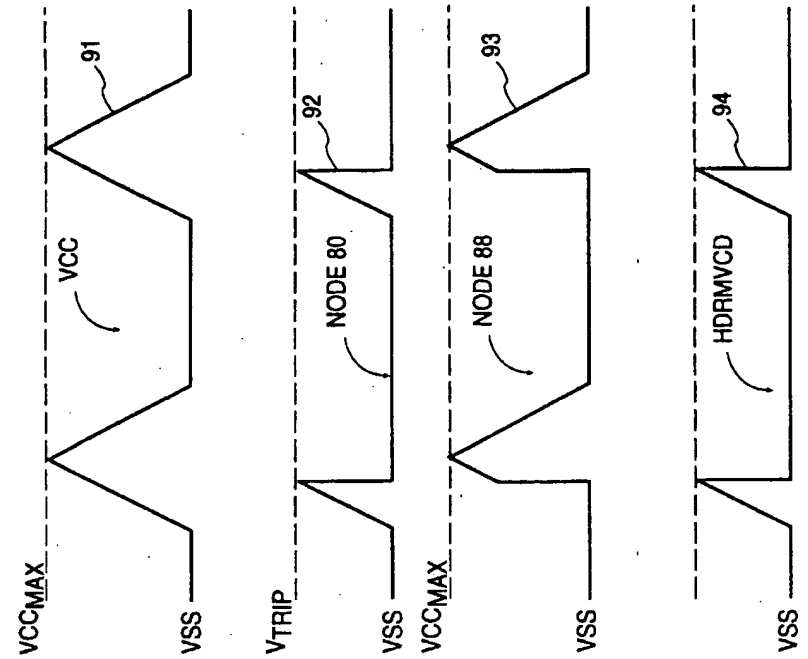

91
VCC
VCCMAX
VSS
92
NODE 80
VTRIP
VSS
93
NODE 88
VCCMAX
VSS
94
HDRMVCD
VSS

FIG. 5

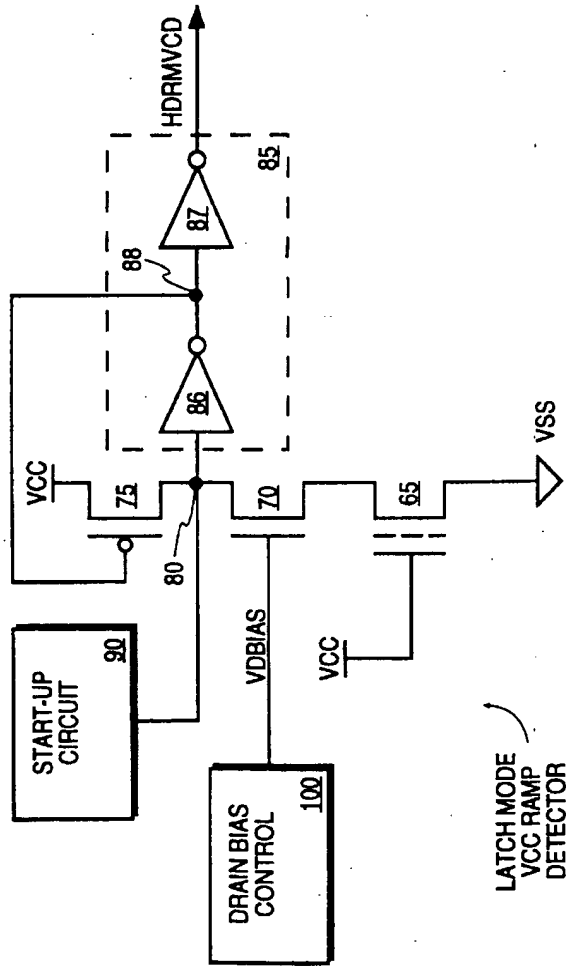

HDRMVCD
85
87
88
86
VCC
75
80
70
65
VSS
START-UP CIRCUIT
90
VDBIAS
VCC
DRAIN BIAS CONTROL
100
LATCH MODE VCC RAMP DETECTOR
30

FIG. 4

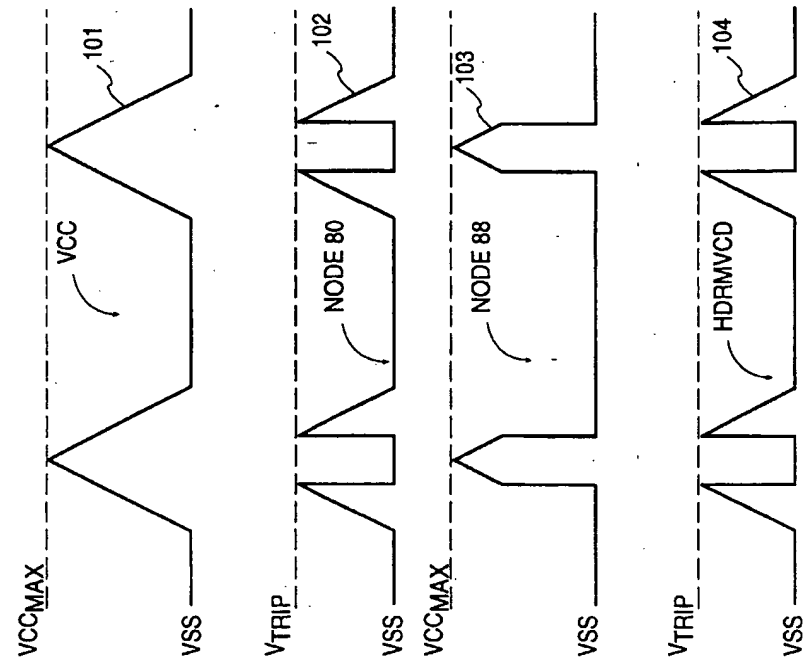

101
VCC
VCCMAX
VSS
102
NODE 80
VTRIP
VSS
103
NODE 88
VCCMAX
VSS
104
HDRMVCD
VTRIP
VSS

FIG. 7

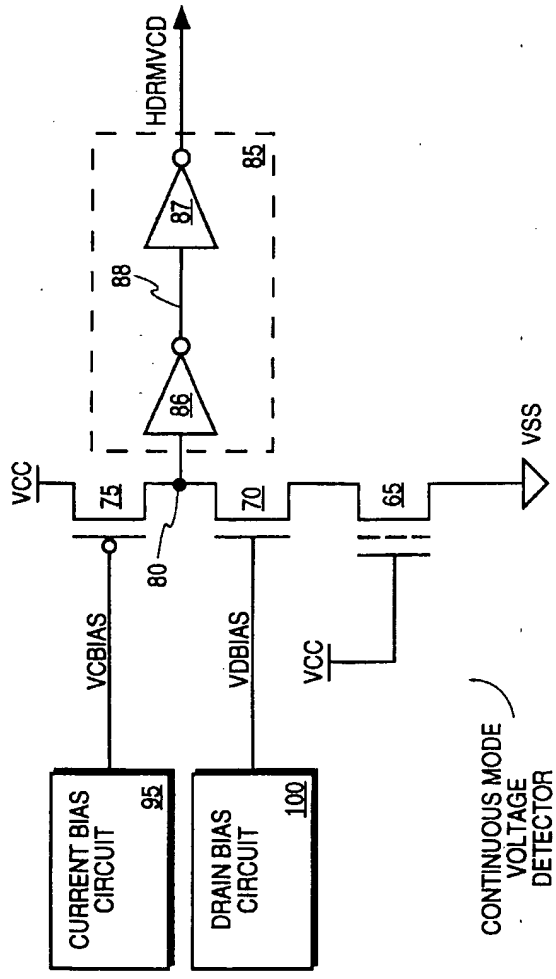

HDRMVCD
85
87
88
86
VCC
75
80
70
65
VSS
VCBIAS
VDBIAS
VCC
CURRENT BIAS CIRCUIT 95
DRAIN BIAS CIRCUIT 100
CONTINUOUS MODE VOLTAGE DETECTOR 96

FIG. 6

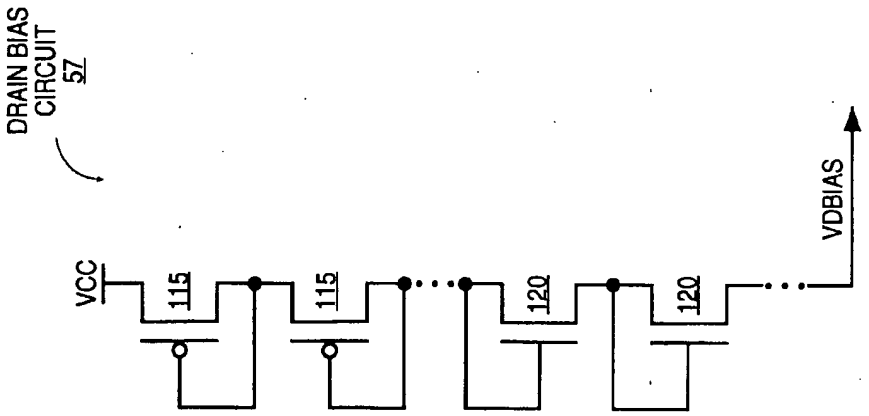

DRAIN BIAS CIRCUIT 57
VCC
115
115
120
120
VDBIAS

FIG. 9

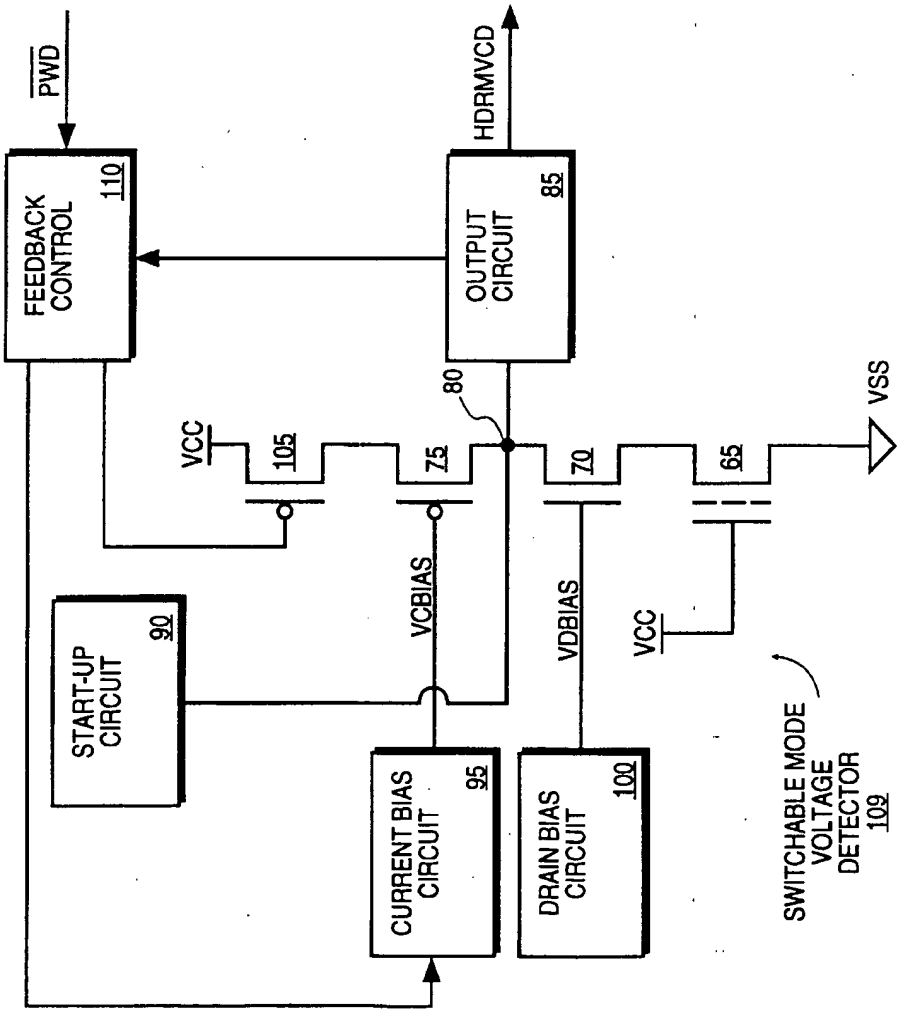

PWD
FEEDBACK CONTROL 110
HDRMVCD
OUTPUT CIRCUIT 85
80
VSS
VCC
105
75
70
65
VCBIAS
VDBIAS
VCC
START-UP CIRCUIT 90
CURRENT BIAS CIRCUIT 95
DRAIN BIAS CIRCUIT 100
SWITCHABLE MODE VOLTAGE DETECTOR 109

FIG. 8

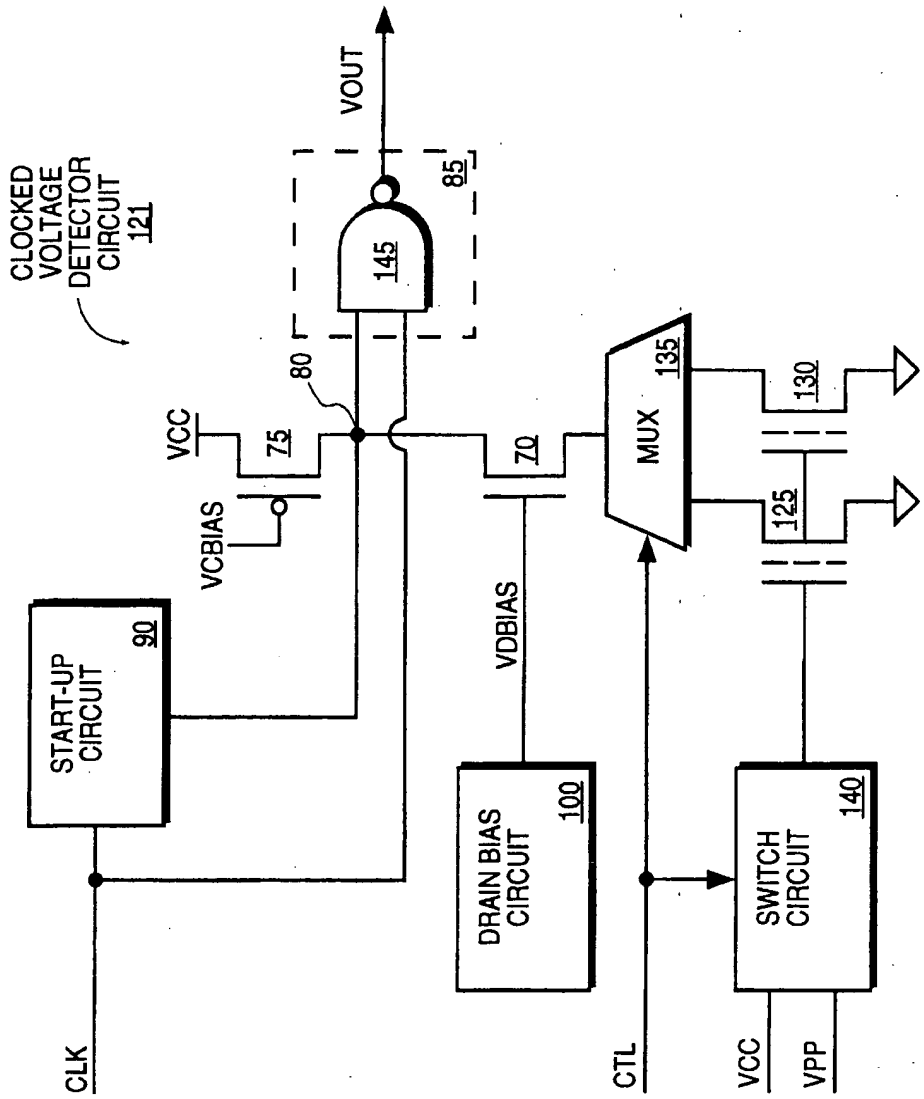

CLOCKED VOLTAGE DETECTOR CIRCUIT 121
VOUT
85
145
80
VCC
75
VCBIAS
70
MUX
135
130
125
START-UP CIRCUIT
90
VDBIAS
DRAIN BIAS CIRCUIT
100
SWITCH CIRCUIT
140
CLK
CTL
VCC
VPP

FIG. 10

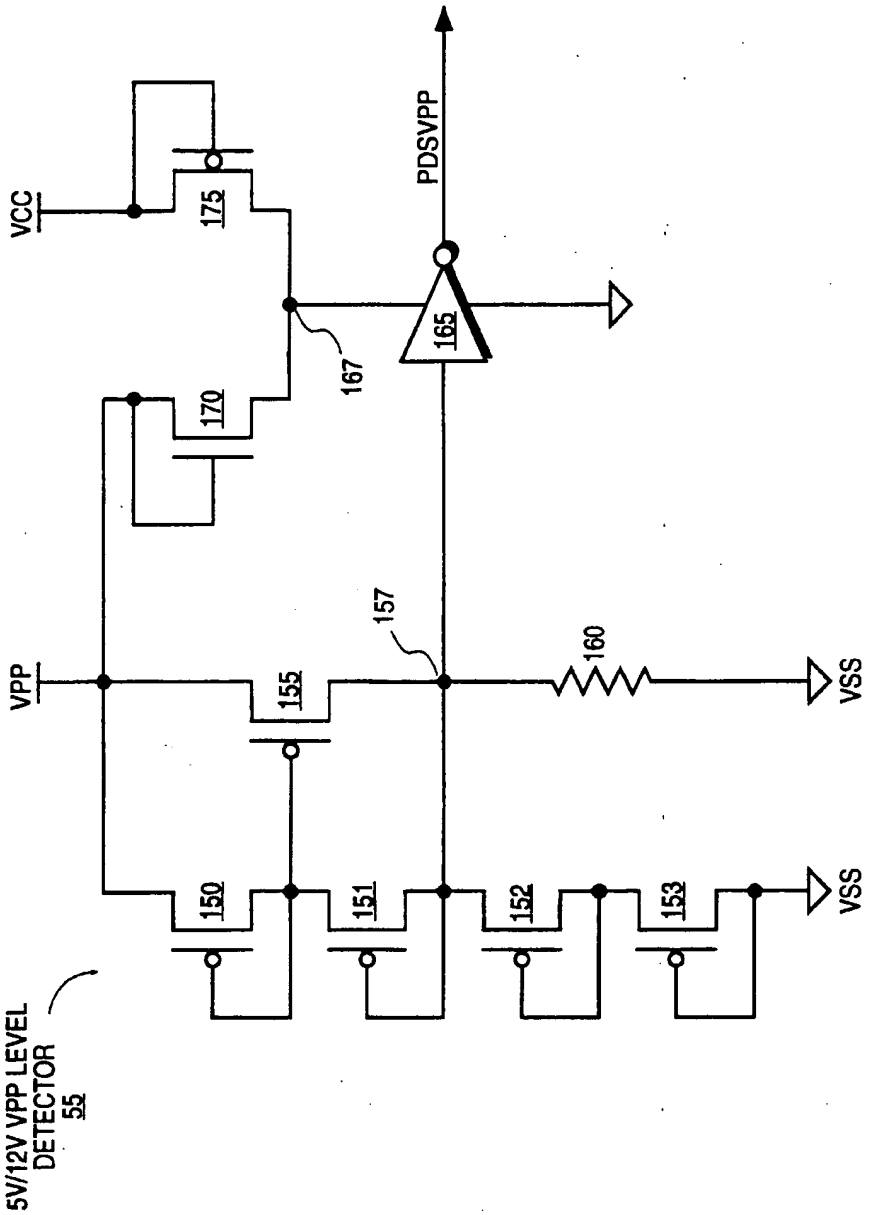

PDSVPP
VCC
175
165
167
170
157
160
VPP
155
VSS
150
151
152
153
VSS
5V/12V VPP LEVEL
DETECTOR
55

FIG. 11

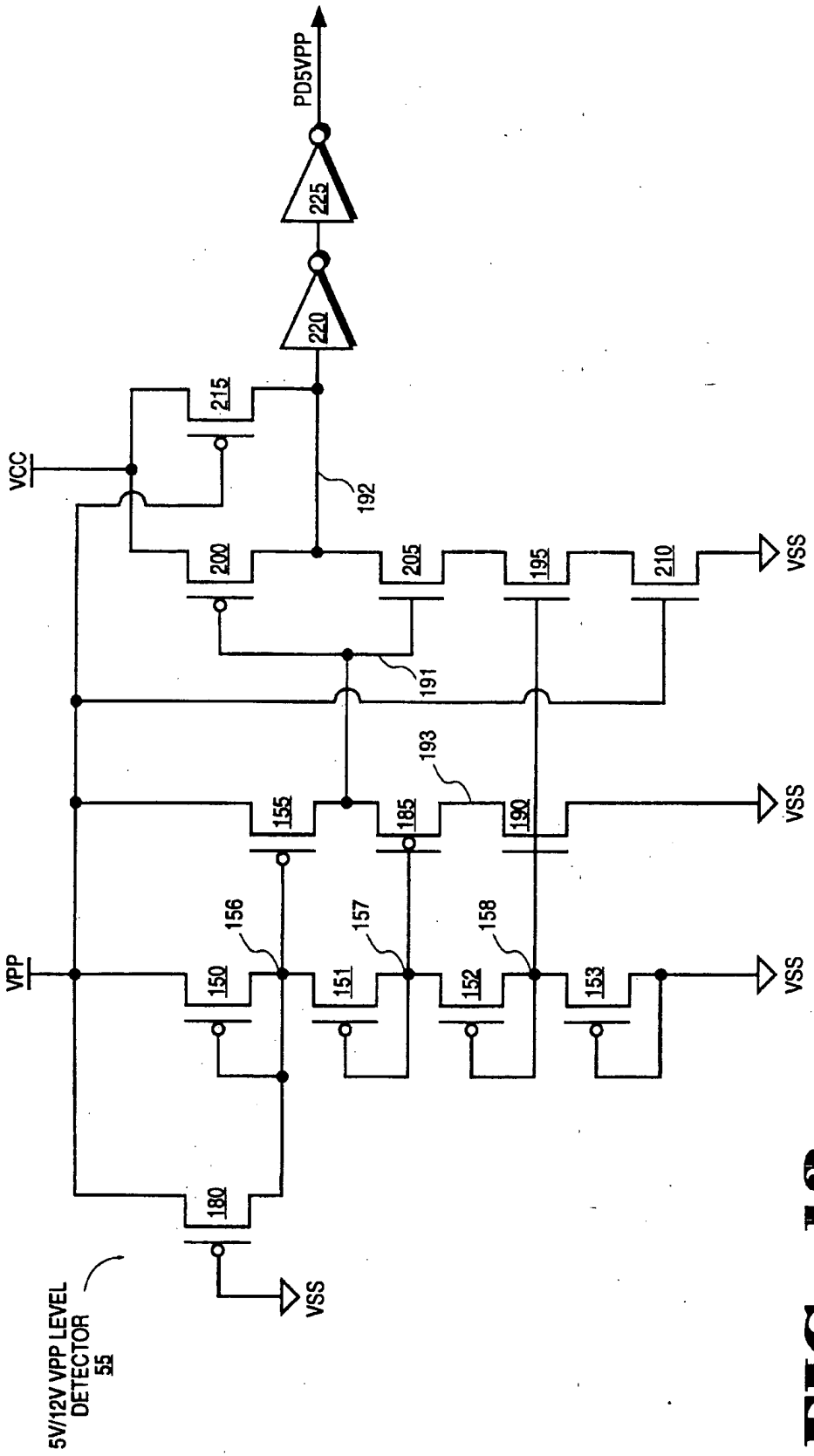

PD5VPP
225
220
215
VCC
192
200
205
195
210
VSS
191
193
155
185
190
VSS
156
157
158
VPP
150
151
152
153
VSS
180
VSS
5V/12V VPP LEVEL DETECTOR 55

FIG. 12

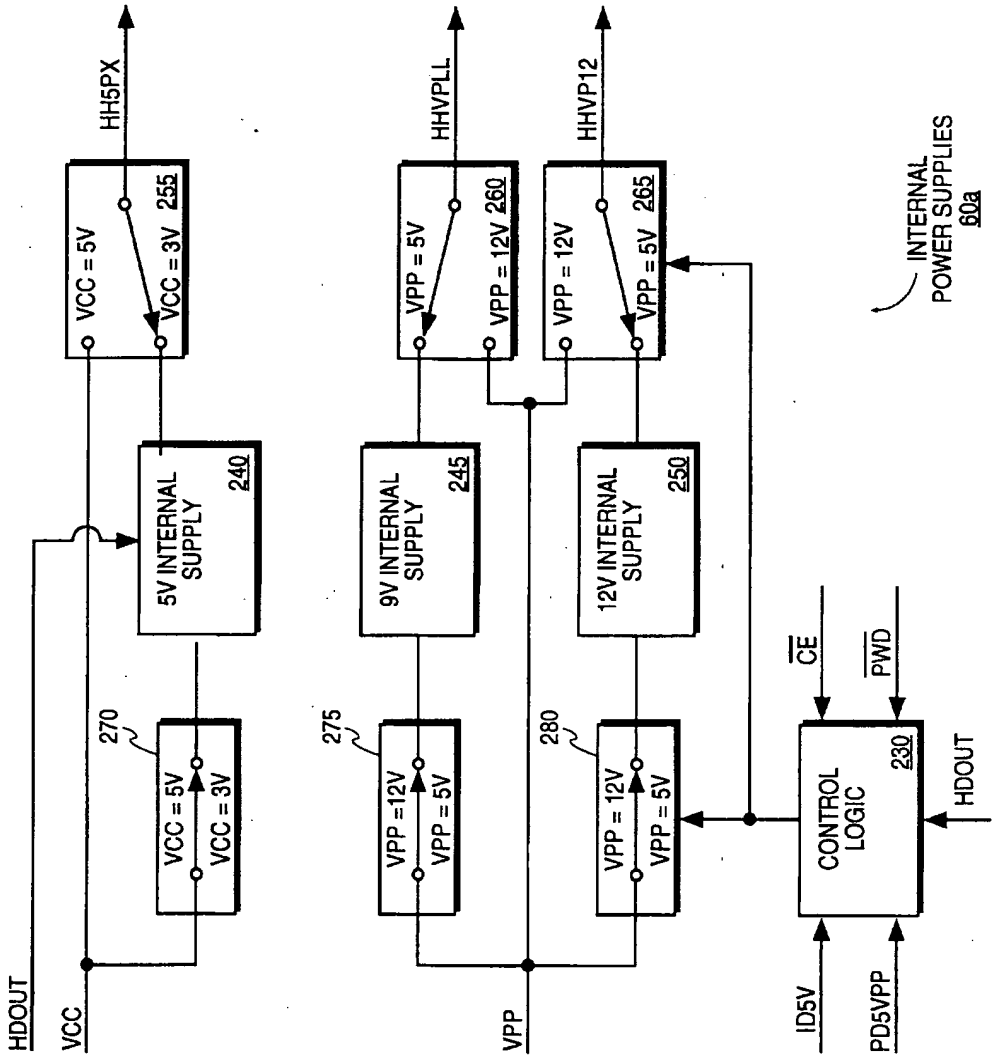

HH5PX
HHVPLL
HHVP12
INTERNAL POWER SUPPLIES 60a
VCC = 5V
VCC = 3V 255
VPP = 5V
VPP = 12V 260
VPP = 12V
VPP = 5V 265
5V INTERNAL SUPPLY 240
9V INTERNAL SUPPLY 245
12V INTERNAL SUPPLY 250
270
275
280
VCC = 5V
VCC = 3V
VPP = 12V
VPP = 5V
VPP = 12V
VPP = 5V
CE
PWD
CONTROL LOGIC 230
HDOUT
HDOUT
VCC
VPP
ID5V
PD5VPP

FIG. 13A

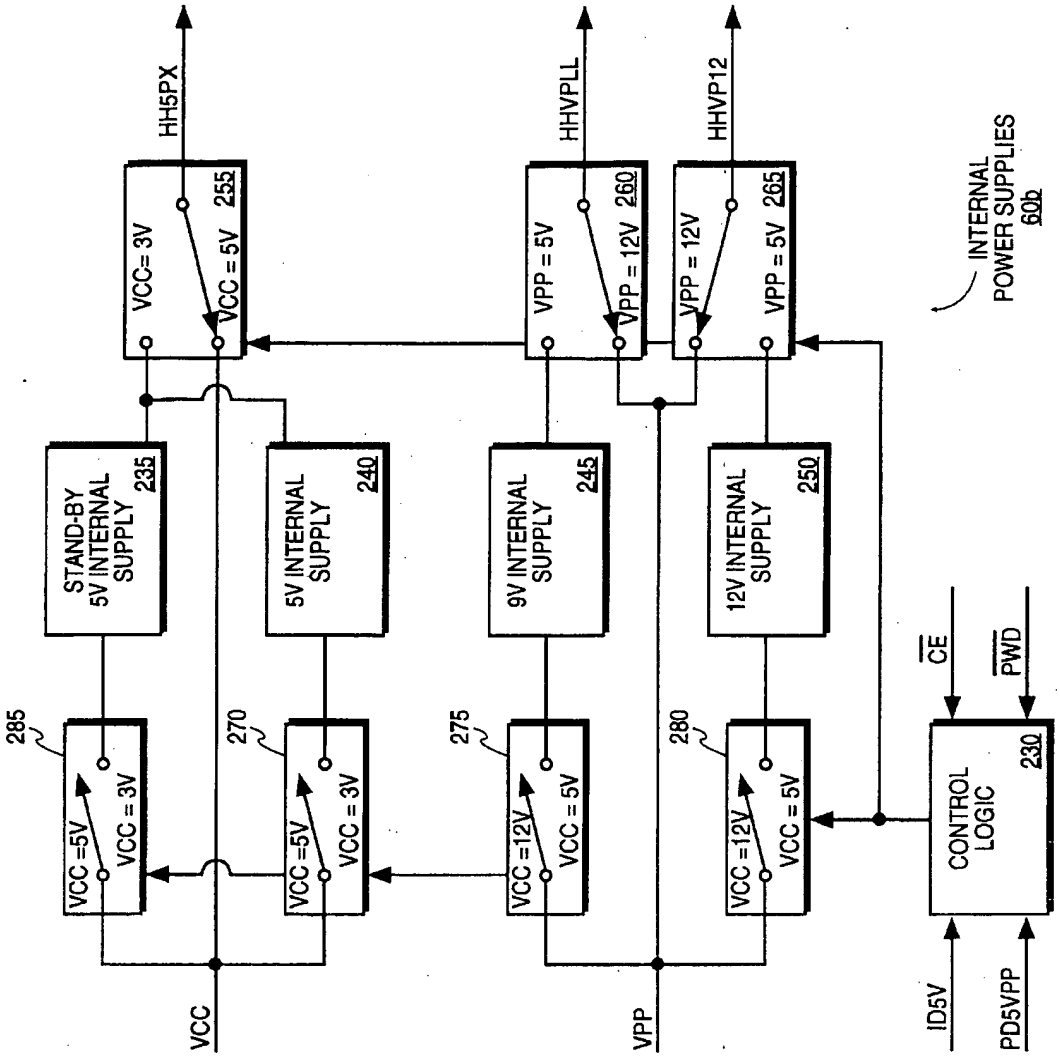

HH5PX
HHVPLL
HHVP12
INTERNAL POWER SUPPLIES 60b
VCC= 3V
VCC = 5V 255
VPP = 5V
VPP = 12V 260
VPP = 12V
VPP = 5V 265
STAND-BY 5V INTERNAL SUPPLY 235
5V INTERNAL SUPPLY 240
9V INTERNAL SUPPLY 245
12V INTERNAL SUPPLY 250
285
270
275
280
VCC =5V
VCC = 3V
VCC =12V
VCC = 5V
CE
PWD
CONTROL LOGIC 230
ID5V
PD5VPP
VCC
VPP

FIG. 13B

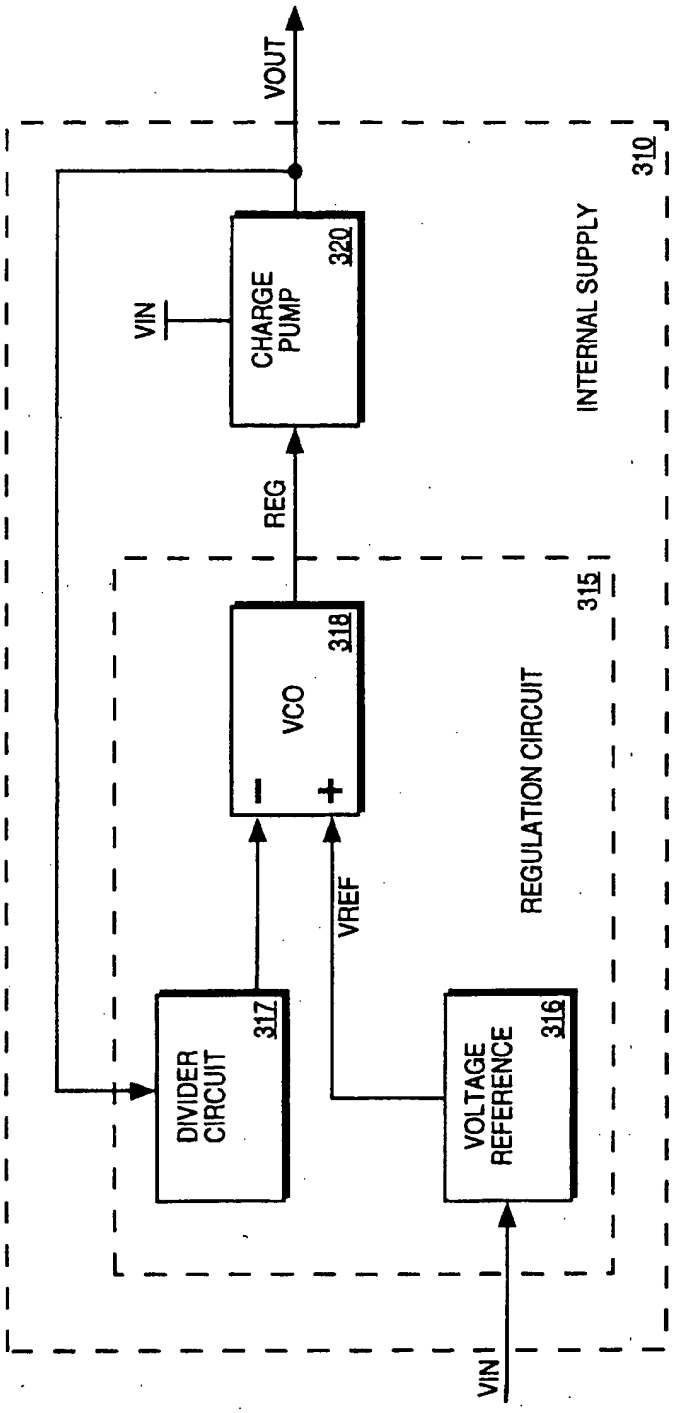

VOUT
310
INTERNAL SUPPLY
VIN
CHARGE PUMP
320
REG
315
REGULATION CIRCUIT
VCO
318
VREF
DIVIDER CIRCUIT
317
VOLTAGE REFERENCE
316
VIN

FIG. 14

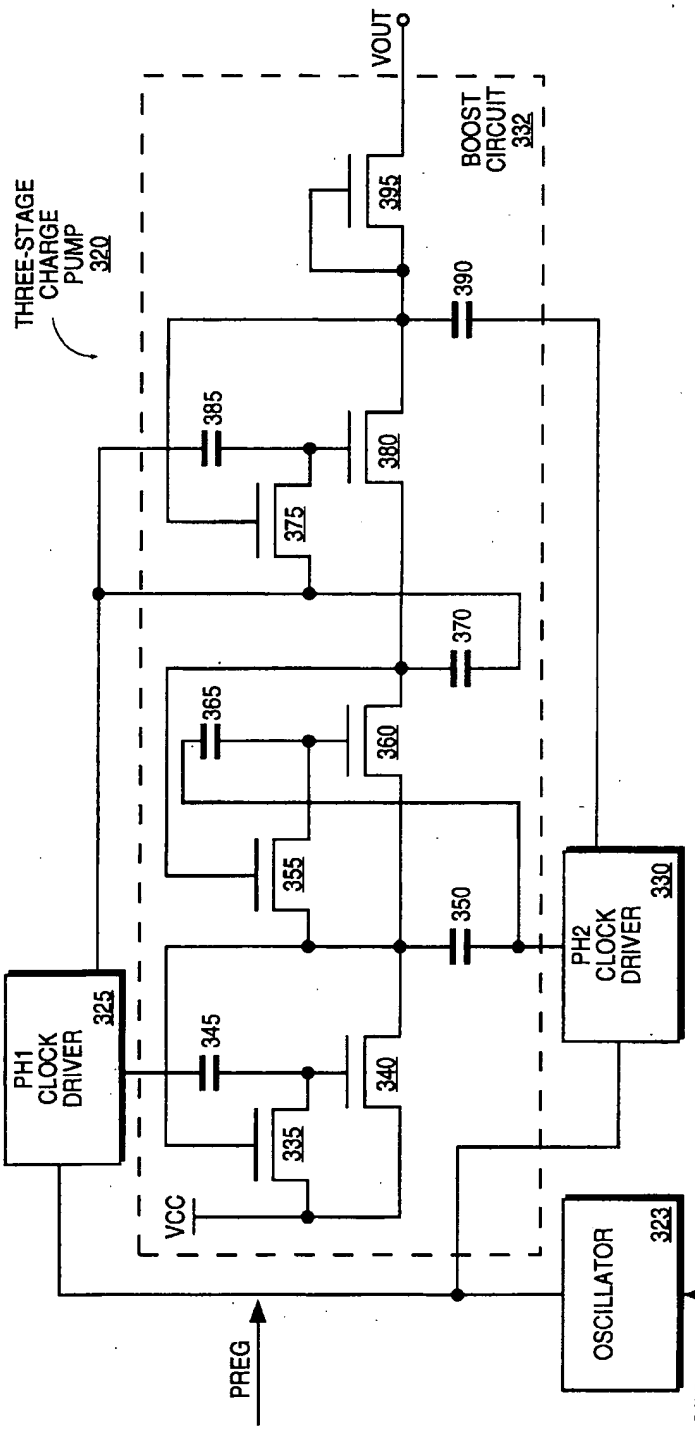

THREE-STAGE CHARGE PUMP 320
BOOST CIRCUIT 332
VOUT
395
390
385
380
375
370
365
360
355
350
345
340
335
PH1 CLOCK DRIVER 325
PH2 CLOCK DRIVER 330
OSCILLATOR 323
VCC
PREG
REG

FIG. 15

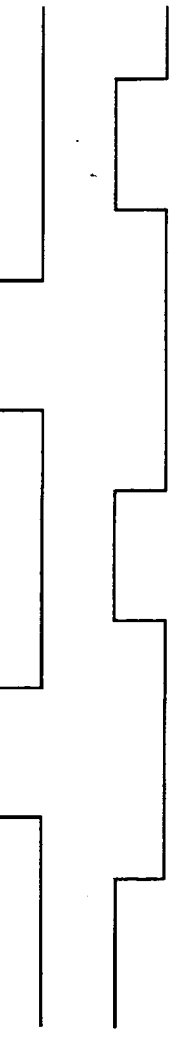

PH1
PH2

FIG. 16

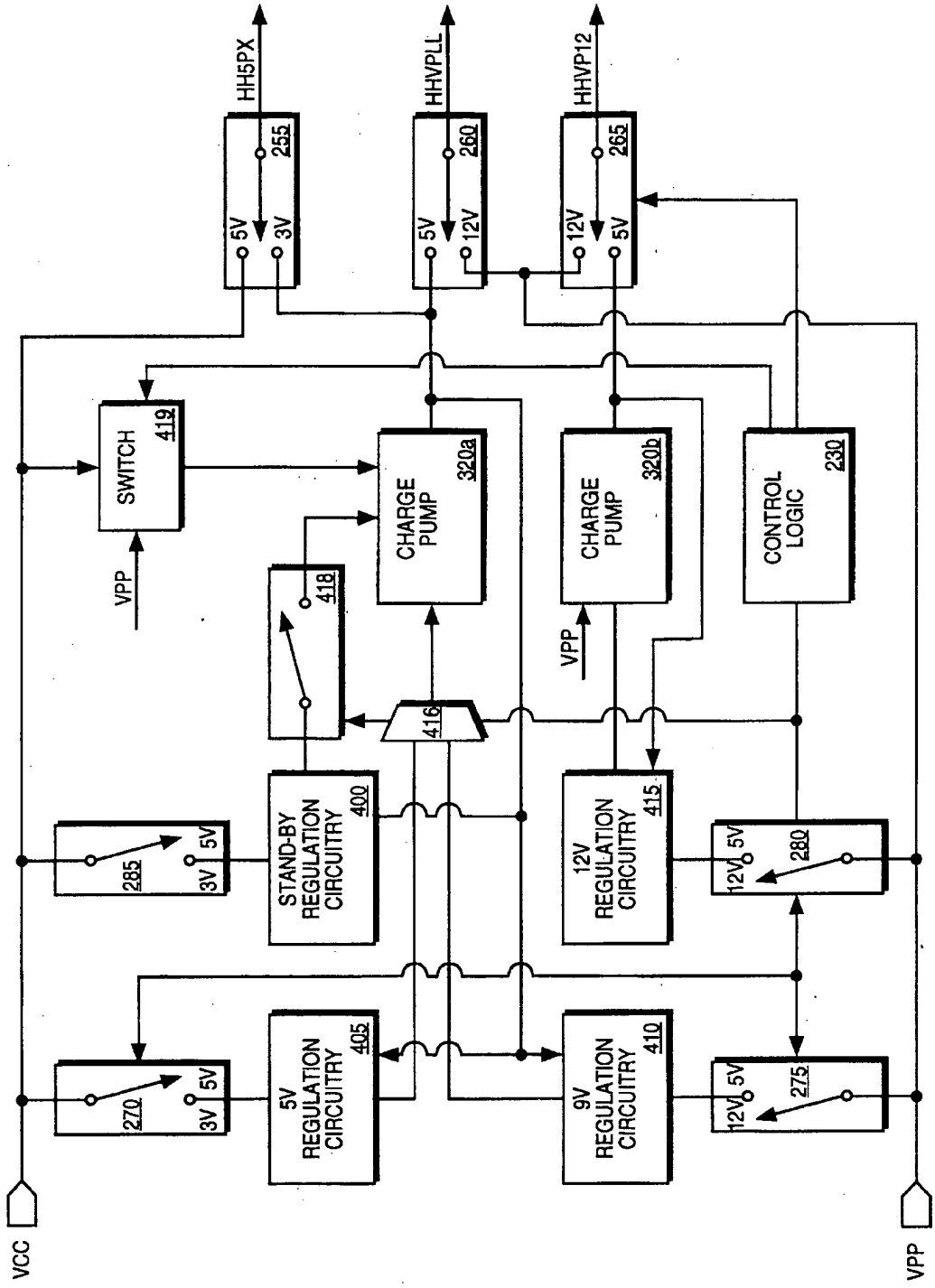

HH5PX
HHVPLL
HHVP12
255
260
265
5V
3V
12V
SWITCH
419
CHARGE PUMP
320a
320b
CONTROL LOGIC
230
VPP
418
416
285
270
STAND-BY REGULATION CIRCUITRY
400
5V REGULATION CIRCUITRY
405
12V REGULATION CIRCUITRY
415
9V REGULATION CIRCUITRY
410
280
275
VCC

FIG. 17

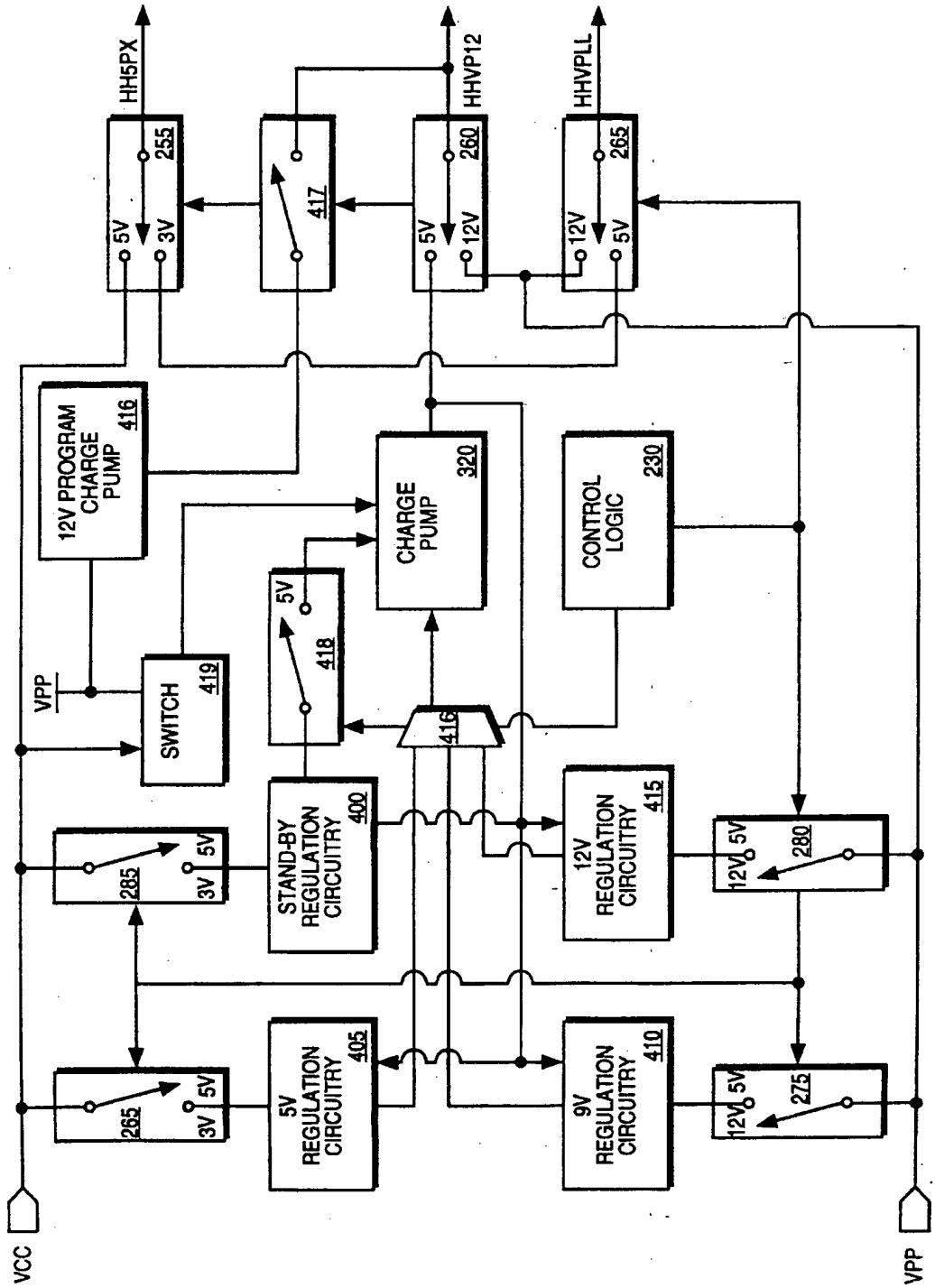

HH5PX
HHVP12
HHVPLL
255
260
265
5V
3V
12V
417
12V PROGRAM CHARGE PUMP 416
CHARGE PUMP 320
CONTROL LOGIC 230
VPP
SWITCH 419
418
416
285
STAND-BY REGULATION CIRCUITRY 400
12V REGULATION CIRCUITRY 415
280
265
5V REGULATION CIRCUITRY 405
9V REGULATION CIRCUITRY 410
275
VCC
VPP

FIG. 18

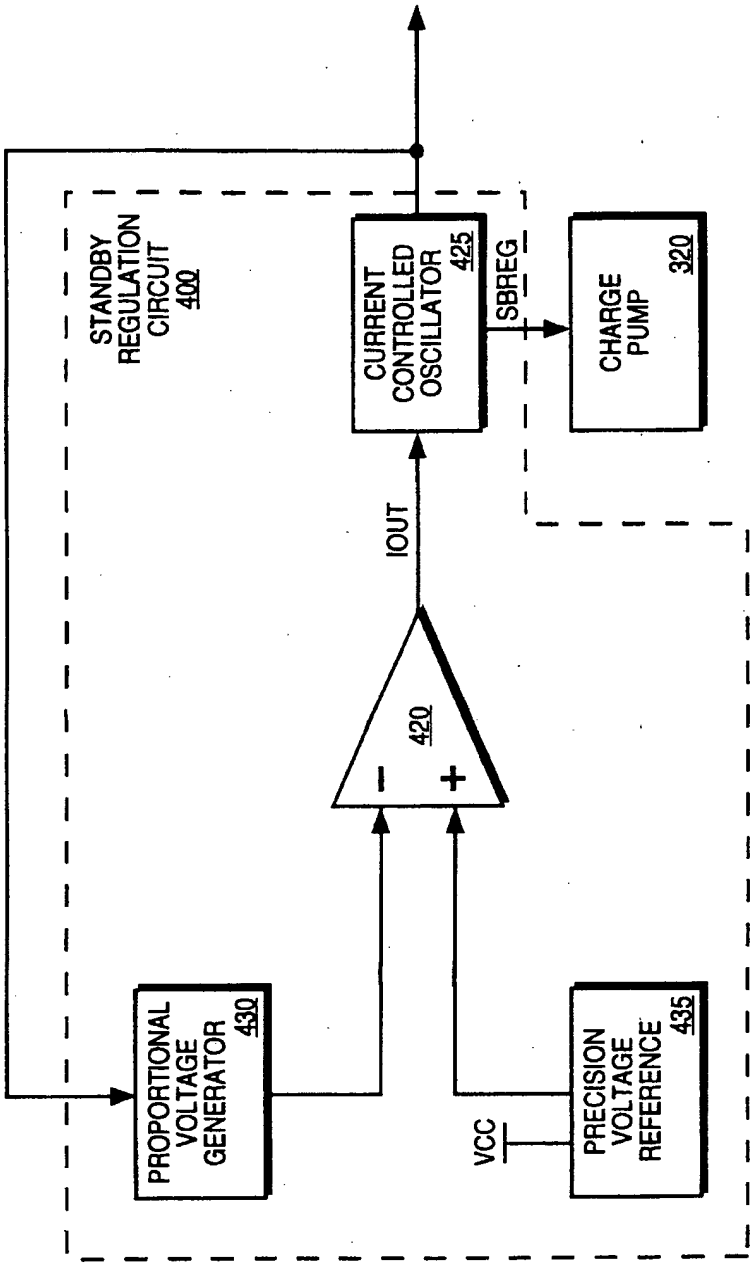

STANDBY REGULATION CIRCUIT 400
CURRENT CONTROLLED OSCILLATOR 425
SBREG
CHARGE PUMP 320
IOUT
420
PROPORTIONAL VOLTAGE GENERATOR 430
VCC
PRECISION VOLTAGE REFERENCE 435

FIG. 19

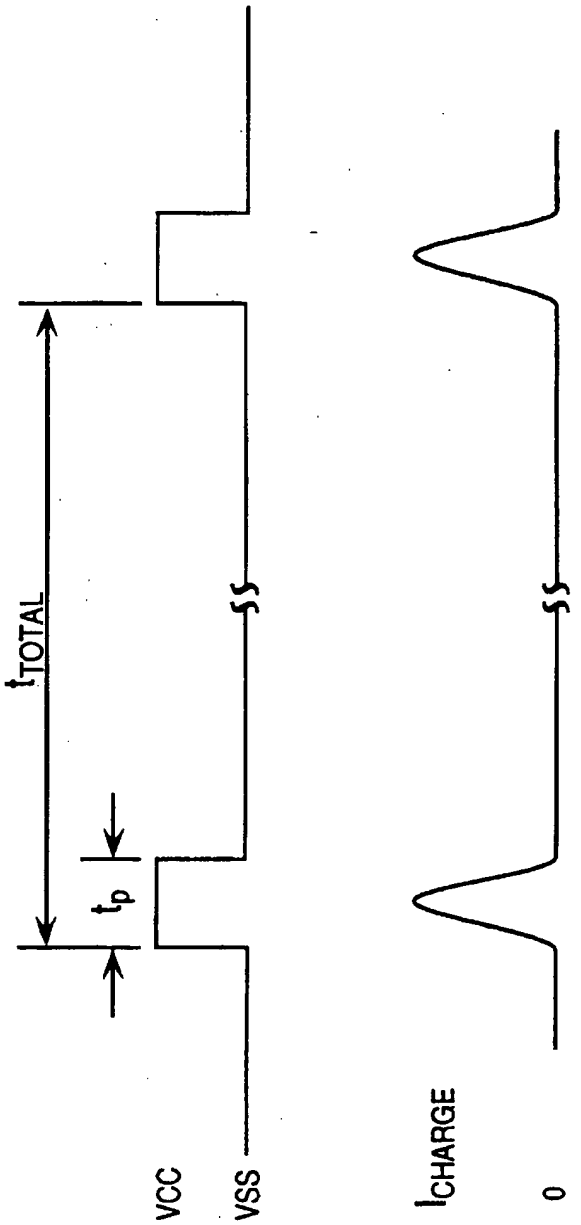


FIG. 20

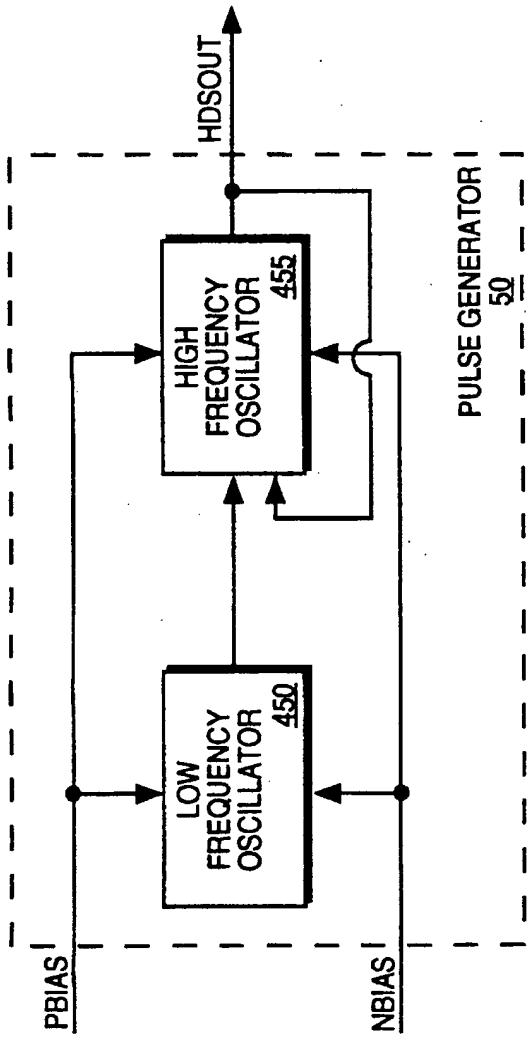

HDSOUT
PULSE GENERATOR
50
HIGH FREQUENCY OSCILLATOR
455
LOW FREQUENCY OSCILLATOR
450
PBIAS
NBIAS

FIG. 21

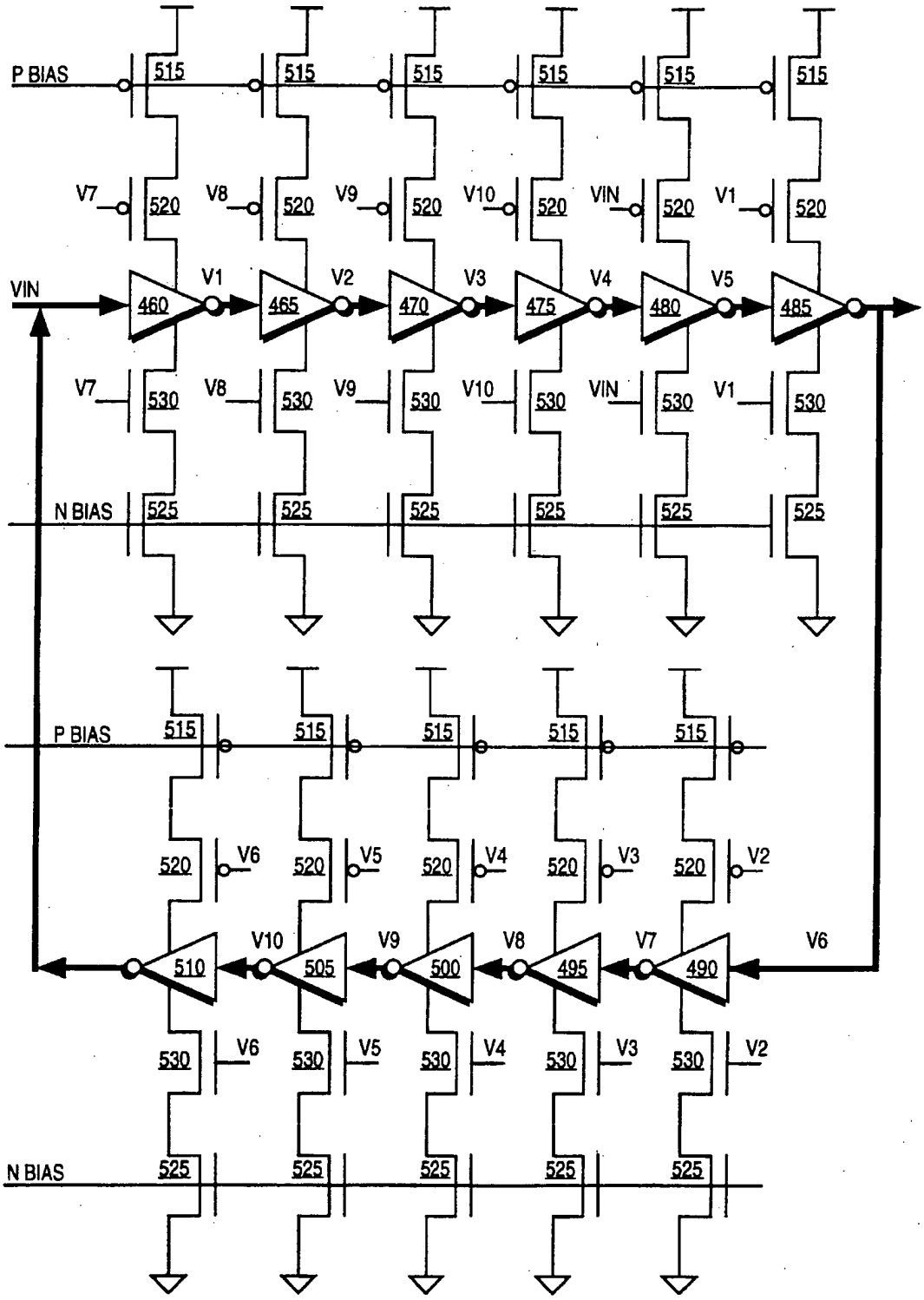

P BIAS
515
V7
520
V8
V9
V10
VIN
V1
VIN
460
V1
465
V2
470
V3
475
V4
480
V5
485
530
N BIAS
525
V6
V5
V4
V3
V2
510
505
500
495
490

FIG. 22

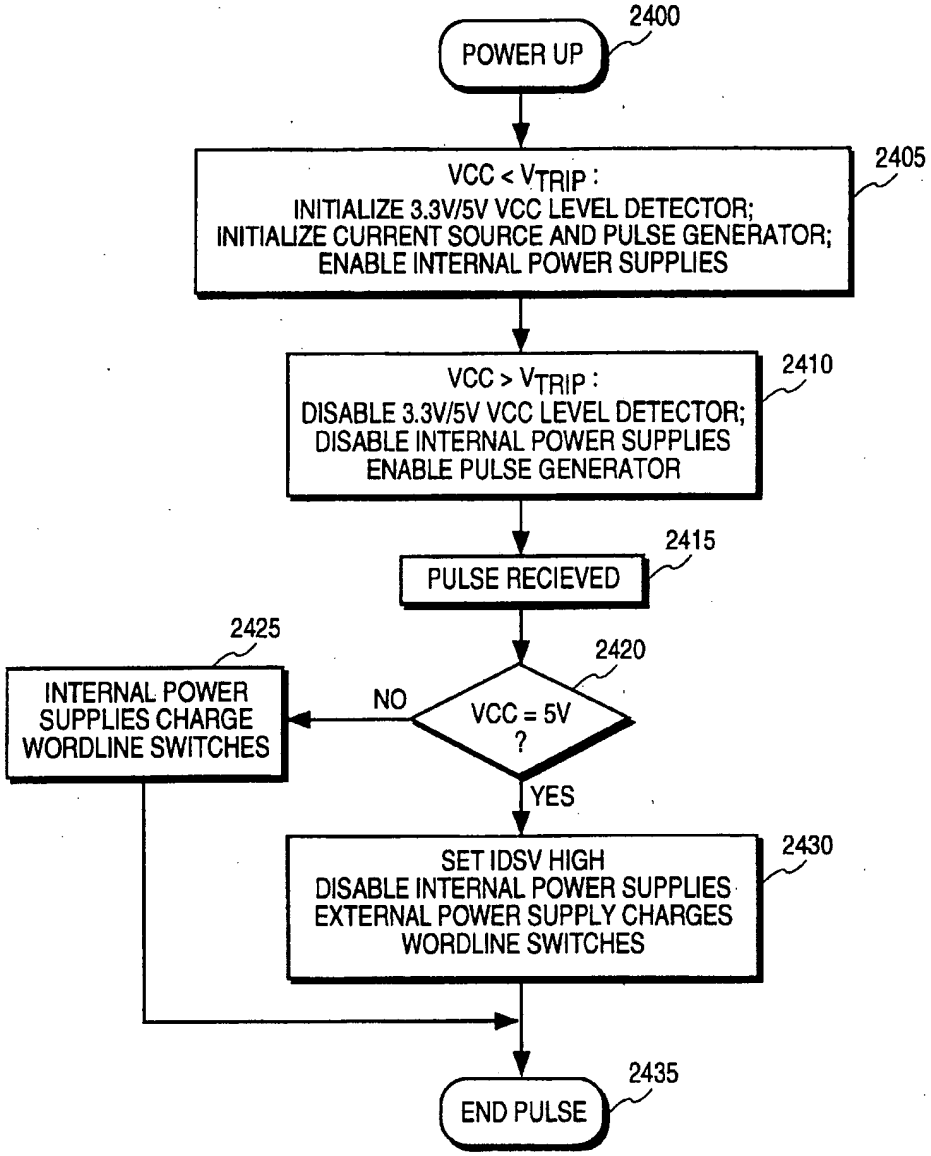

2400
POWER UP
2405
VCC < VTRIP :
INITIALIZE 3.3V/5V VCC LEVEL DETECTOR;
INITIALIZE CURRENT SOURCE AND PULSE GENERATOR;
ENABLE INTERNAL POWER SUPPLIES
2410
VCC > VTRIP :
DISABLE 3.3V/5V VCC LEVEL DETECTOR;
DISABLE INTERNAL POWER SUPPLIES
ENABLE PULSE GENERATOR
2415
PULSE RECIEVED
2420
VCC = 5V
?
NO
2425
INTERNAL POWER
SUPPLIES CHARGE
WORDLINE SWITCHES
YES
2430
SET IDSV HIGH
DISABLE INTERNAL POWER SUPPLIES
EXTERNAL POWER SUPPLY CHARGES
WORDLINE SWITCHES
2435
END PULSE

FIG. 23A

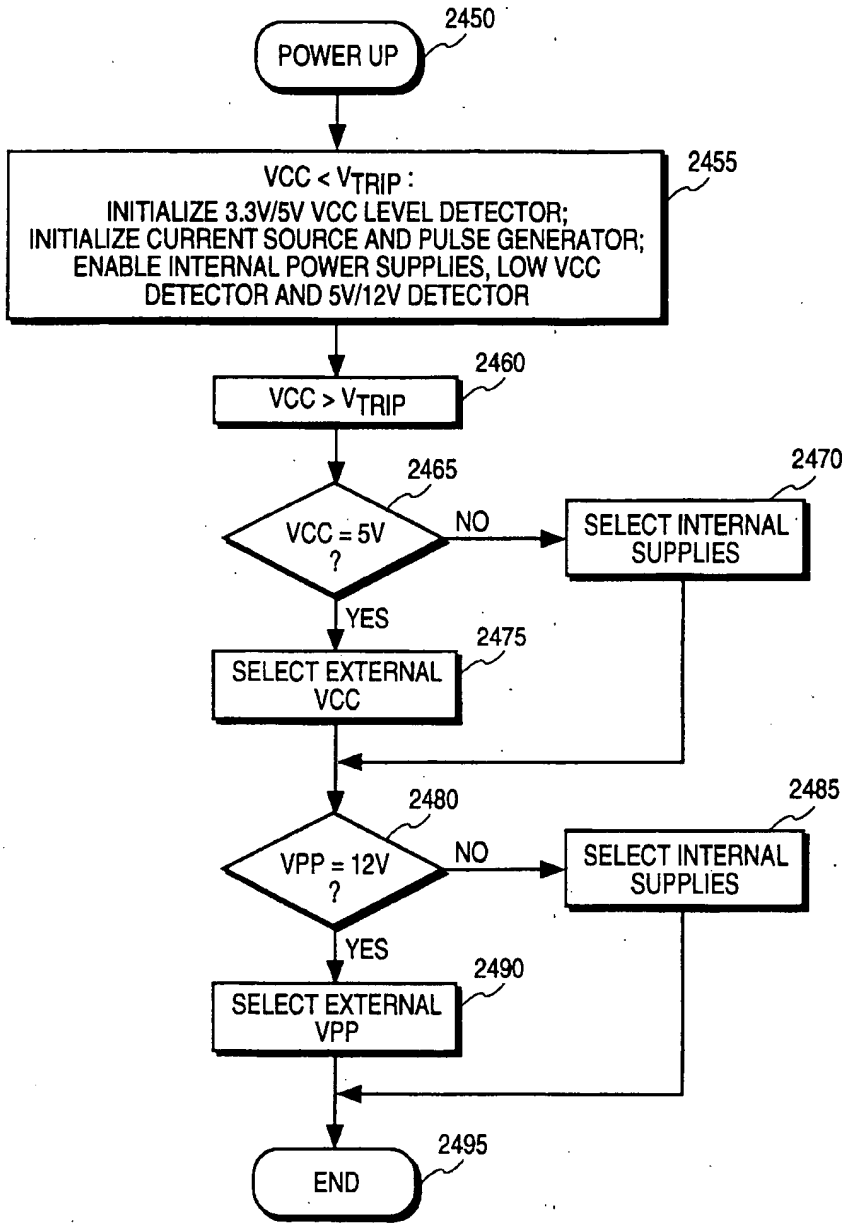

2450
POWER UP
2455
VCC < VTRIP :
INITIALIZE 3.3V/5V VCC LEVEL DETECTOR;
INITIALIZE CURRENT SOURCE AND PULSE GENERATOR;
ENABLE INTERNAL POWER SUPPLIES, LOW VCC
DETECTOR AND 5V/12V DETECTOR
2460
VCC > VTRIP
2465
VCC = 5V
?
NO
2470
SELECT INTERNAL
SUPPLIES
YES
2475
SELECT EXTERNAL
VCC
2480
VPP = 12V
?
NO
2485
SELECT INTERNAL
SUPPLIES
YES
2490
SELECT EXTERNAL
VPP
2495
END

FIG. 23B

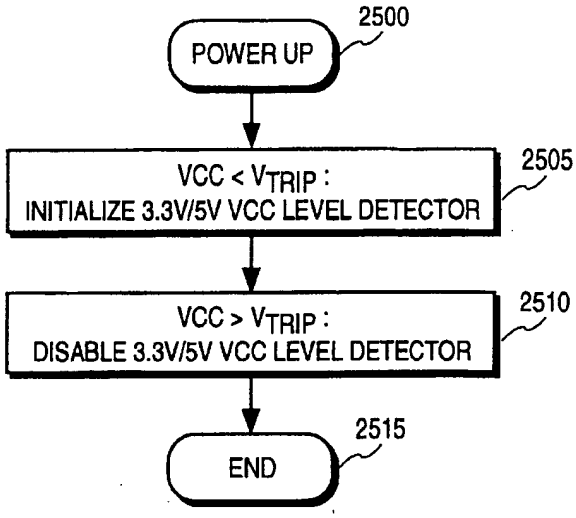

2500
POWER UP
VCC < V_{TRIP} :
INITIALIZE 3.3V/5V VCC LEVEL DETECTOR
2505
VCC > V_{TRIP} :
DISABLE 3.3V/5V VCC LEVEL DETECTOR
2510
END
2515

FIG. 24A

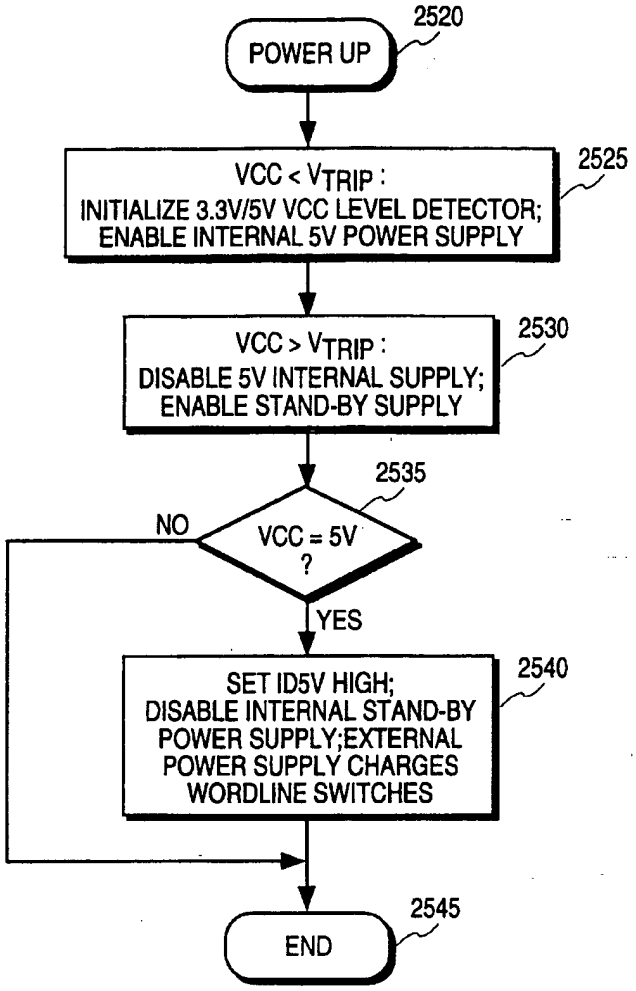

2520
POWER UP
2525
VCC < V_{TRIP} :
INITIALIZE 3.3V/5V VCC LEVEL DETECTOR;
ENABLE INTERNAL 5V POWER SUPPLY
2530
VCC > V_{TRIP} :
DISABLE 5V INTERNAL SUPPLY;
ENABLE STAND-BY SUPPLY
2535
NO
VCC = 5V
?
YES
2540
SET ID5V HIGH;
DISABLE INTERNAL STAND-BY
POWER SUPPLY;EXTERNAL
POWER SUPPLY CHARGES
WORDLINE SWITCHES
2545
END

FIG. 24B

CHARGE PUMP CIRCUIT FOR PROVIDING MULTIPLE OUTPUT VOLTAGES FOR FLASH MEMORY

The present invention relates generally to power management of integrated circuits and more particularly to the power management of nonvolatile memory devices.

BACKGROUND

The use of computer systems has grown so pervasive that the power consumed by computer systems has become a concern for computer system designers and consumers. To reduce the cost of providing power to operate computer systems and the corresponding consumption of energy resources, the goal of designing a "green PC" that consumes less power has been pursued by several manufacturers. Manufacturers of mobile or "portable" computer systems that operate using rechargeable batteries as power supplies have also attempted to reduce power consumption so that the mobile computer system may be used for extended periods of time without recharging the batteries.

To reduce power consumption and to extend battery life, much of the integrated circuitry used as components of computer systems is being designed to operate at low voltage levels. For example, the circuitry and components used in portable computers are being designed to operate exclusively at voltage levels such as five volts and 3.3 volts. This reduces power consumption and allows more components to be placed closer to one another in the circuitry.

Unfortunately, the movement towards reducing the power consumption of computer systems may conflict with the desire to provide after-market upgrades and add-on devices for portable computer systems. One type of device that may be used to increase the versatility of a portable computer system is the flash electrically erasable programmable read only memory ("flash EEPROM"). Flash EEPROMs are nonvolatile memory devices that can be programmed and erased by the user, and flash EEPROMS may be used, for example, as BIOS ROMs or as part of a plug-in memory card. Flash EEPROMs typically require higher voltages for programming and erasing data than can be provided directly by the reduced voltage power supplies of green PCs and portable computers.

One solution for allowing flash EEPROMs to be used in reduced voltage computer system designs is to provide charge pump circuits external to the flash EEPROMs for boosting the supply voltage levels of the computer system to the higher voltage levels required by the flash EEPROM. A difficulty with this solution is that the use of separate charge pump circuits requires printed circuit board space that may be at a premium in a portable computer system.

An alternative solution is to design flash EEPROMs that include charge pump circuits for internally generating the higher voltage levels required by the flash EEPROM. One difficulty with this solution is that charge pumps internal to the flash EEPROM require semiconductor die space, which may require an increase in the semiconductor die size for the flash EEPROM. Another difficulty is that internal charge pump circuits may not be able to provide sufficient current to program and erase the memory cell array as quickly as external charge pumps, and operation of the flash EEPROM may be slowed.

SUMMARY AND OBJECTS OF THE INVENTION

Therefore, one object of the present invention is to provide internal power supplies such that the need for external charge pumps reduced.

Another object of the present invention is to provide internal power supply circuits that require a reduced amount of semiconductor die space.

These and other objects of the present invention are provided by a circuit for generating one of a plurality of output voltages. The circuit includes a first conductor coupled to a first supply voltage, a second conductor coupled to a second supply voltage, a charge pump having an input and an output, a multiplexor, a first regulation circuit, and a second regulation circuit. The first regulation circuit is coupled to the first input of the multiplexor and the output of the charge pump. The first regulation circuit is for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first output voltage when the first input of the multiplexor is coupled to the output of the multiplexor. The second regulation circuit is coupled to the second input of the multiplexor and the output of the charge pump. The second regulation circuit is for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second output voltage when the second input of the multiplexor is coupled to the output of the multiplexor. The multiplexing of the regulation circuitry results in a reduced number of components.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

FIG. **1** shows a computer system that includes one or more components having novel circuitry.

FIG. **2** shows a flash EEPROM that includes novel circuitry.

FIGS. **3A** and **3B** show smart voltage circuitry of the flash EEPROM according to different embodiments.

FIG. **4** shows a latch mode VCC detector.

FIG. **5** shows the behavior of the latch mode VCC detector.

FIG. **6** shows a continuous mode VCC detector.

FIG. **7** shows the behavior of the continuous mode VCC detector.

FIG. **8** shows a VCC detector capable of operating in both the latch mode and the continuous mode.

FIG. **9** shows a drain bias control circuit for the VCC detector in more detail.

FIG. **10** shows a clocked voltage detector circuit.

FIG. **11** shows one 5/12 v VPP level detector circuit.

FIG. **12** shows a second 5/12 v VPP level detector circuit.

FIGS. **13A** and **13B** show internal power supplies according to different embodiments.

FIG. **14** shows an internal power supply as including regulation circuitry and a charge pump.

FIG. **15** shows a charge pump in more detail.

FIG. **16** shows clock signals that may be provided to the charge pump of FIG. **15**.

FIG. **17** shows the internal power supplies wherein three charge pump circuits share the same charge pump.

FIG. **18** shows the internal power supplies wherein four charge pump circuits share the same charge pump.

FIG. **19** shows the regulation circuitry of a stand-by charge pump.

FIG. **20** shows the output of the pulse generator and the corresponding current consumption of a charge pump enabled in response to a pulse generated by the pulse generator.

FIG. **21** shows the pulse generator circuit in more detail.

FIG. **22** shows an oscillator of the pulse generator circuit that uses subthreshold biasing.

FIG. **23**A and **23**B are flow charts illustrating a method of operation for the flash EEPROM **20** that includes the smart voltage circuitry shown in FIG. **3**A.

FIG. **24**A and **24**B are flow charts illustrating a method of operation for the flash EEPROM **20** that includes the smart voltage circuitry shown in FIG. **3**B.

DETAILED DESCRIPTION

FIG. **1** shows a general purpose computer system **10** that includes a power supply **11**, a central processing unit ("CPU") **12**, a main memory **13**, a read only memory **14**, a mass storage device **15**, a frame buffer **16**, and an input device **17**, all of which are coupled to a bus **19**. The bus **19** includes a data bus and acts as a primary interconnect for the components of the computer system **10** so that data may be transferred among the various components. The computer system **10** also includes a display device **18** that is coupled to the frame buffer **16** for receiving image data for display. The read only memory **14** may be a flash EEPROM, and the mass storage device may be a "solid state disk drive" that includes a plurality of flash EEPROMs for emulating the operation of a magnetic hard disk drive.

The computer system **10** may be a portable computer, a workstation, a minicomputer, a programmable digital assistant ("PDA"), a mainframe, or any other type of computer, and the power requirements of the computer system **10** are defined accordingly. For example, if the computer system **10** is a workstation, the system operating voltage VCC may be 5.0 volts, wherein if the computer system **10** is a portable computer operating from a rechargeable battery, the system operating voltage VCC may be 3.3 volts. It may also be possible that the computer system **10** is a portable computer system that provides different operating voltage levels depending on whether power is supplied by the rechargeable battery or by an AC adapter.

The power supply **11** therefore includes a VCC supply output for supplying the operating voltage VCC of the computer system **10** to the components of the computer system via power conductors of the bus **19**. Wherein the computer system **10** is a portable computer, the power supply **11** may be a rechargeable battery. The power supply **11** may also include a VPP supply output for supplying a twelve volt programming voltage VPP to the read only memory **14** or the mass storage device **15**. If the power supply **11** does not include a separate VPP supply output, the VPP input of flash EEPROMs included in the computer system **10** may be coupled to receive the VCC operating voltage.

The flash EEPROMs of the computer system **10** includes circuitry that allows the flash EEPROMs to operate when VCC is equal to 3.3 volts or 5.0 volts and VPP is equal to 5.0 volts or 12.0 volts. Each flash EEPROM therefore includes circuitry for detecting the supply voltages supplied by the power supply **11**, wherein each flash EEPROM configures itself for operation in response to the detected voltages. Not all the flash EEPROMs of the computer system **10** need to include such circuitry.

FIG. **2** shows a flash EEPROM that includes circuitry for detecting system supply voltages. The flash EEPROM **20** is an integrated circuit that may be formed on a single semiconductor substrate and that typically includes a memory cell array **21** comprising a plurality of flash memory cells **22**, each of which is a floating gate transistor device having a select gate, a floating gate, a drain, and a source. The flash memory cells **22** of the memory cell array **21** are arranged in a matrix of rows and columns, wherein a common "wordline" is coupled to the select gate of each flash memory cell of a row and a common "bitline" is coupled to the drain of each flash memory cell of a column.

A flash memory cell **22** is programmed by placing excess charge on the floating gate, which increases the threshold voltage V_t of the flash memory cell **22**. The flash memory cell **22** may be placed in two or more analog states that can be represented by one or more bits. Programming may be accomplished by applying 12.0 volts to the gate, 6.0 volts to the drain, and grounding the source such that electrons are placed on the floating gate by hot electron injection. The flash memory cell **22** is erased by removing the excess charge from the floating gate, and erasure may be accomplished by applying 12.0 volts to the source, grounding the gate, and allowing the drain to float such that electrons are removed from the floating gate via electron tunneling. It is possible to erase several flash memory cells simultaneously, and the operation of erasing several flash memory cells simultaneously is known as a "block erase."

To determine whether the flash memory cell **22** is in the erased state or in a programmed state, a constant voltage is applied to the select gate of the flash memory cell to sense the amount of drain-source current I_{DS} for the flash memory cell **22**. Such a read operation may be accomplished by applying 5.0 volts to the gate, grounding the source, and applying 1.0 volt to the drain. To perform read, program, and erase operations on a selected set of flash memory cells, the flash EEPROM **20** includes wordline switches and decoders **23**, source switches and decoders **24**, and bitline switches and decoders **25**, all of which are controlled by the control engine **26** to select the desired flash memory cells and to apply the appropriate voltages to the selected flash memory cells. The smart voltage circuitry **27** is coupled to the VCC and VPP input pins of the flash EEPROM **20** and is used to supply the required voltages to the wordline switches and decoders **23**, the source switches and decoders **24**, and the bitline switches and decoders **25** in response to the detected supply levels and the mode of operation for the flash EEPROM **20**.

The smart voltage circuitry **27** includes internal power supplies (shown in FIGS. **3**A and **3**B) that may be selected to supply the necessary voltages for operating the flash EEPROM if the external supply levels are determined to be less than the required values for programming, erasing, or reading the memory cell array **21**. For example, an internal power supply may be enabled to supply a 5.0 volt output if the external operating supply voltage VCC is detected to be at 3.3 volts, but if the external operating supply voltage VCC is detected to be at 5.0 volts, the internal power supply is disabled and the external operating supply voltage VCC is delivered to the memory cell array **21**. Similarly, an internal power supply may be enabled during programming and erase operations to supply a 12.0 volt output if the external programming supply voltage VPP is detected to be at 5.0 volts, but if the external programming supply voltage VPP

is detected to be at 12.0 volts the internal power supply is disabled and the external programming supply voltage VPP is delivered to the memory cell array.

The smart voltage circuitry **27** thus allows the same flash EEPROM **20** to be used in computer systems that operate at either high or low voltages. Wherein printed circuit board space is at a premium, the system designer can use the internal power supplies of the flash EEPROM **20** to provide the voltages required for programming and erasing, and an external charge pump circuit is not required. Alternatively, wherein memory performance is at a premium, the system designer can use a power supply or external charge pump circuit to provide the programming and erase voltages.

The smart voltage circuitry **27** may find application for many different types of integrated circuits and more particularly memory devices. For example, the smart voltage circuitry described herein may be used in dynamic random access memories (DRAMs), erasable programmable read only memories (EPROMs), and electrically erasable programmable read only memories (E^2PROMs). The smart voltage circuitry **27** may also be used to detect and select the voltages for the different modules of a multi-chip module. The internal power supplies may be provided as one module, and the voltage detection and selection circuitry may be provided as a second module. The voltage detection and selection circuitry can be used to detect the external power supply voltages and selectively enable the appropriate outputs of the internal power supplies, if necessary.

The flash EEPROM **20** has three modes of operation, including an active mode, a stand-by mode, and a deep power down mode. The stand-by and deep power down modes are both reduced power modes. To define the mode of operation of the flash EEPROM **20**, the control engine **26** receives the control signals chip enable $\overline{CE}$, output enable $\overline{OE}$, write enable $\overline{WE}$, and power down $\overline{PWD}$. Chip enable signal $\overline{CE}$ is the power control and is used for device selection of the flash EEPROM **20**. The output enable signal $\overline{OE}$ is the output control for flash EEPROM **20** and is used to gate data from the output pins from flash EEPROM **20**, dependent on device selection. Both of the control signals $\overline{CE}$ and $\overline{OE}$ must be at a logic low level to obtain data at the outputs of flash EEPROM **20**. The write enable signal $\overline{WE}$ allows writes to control engine **26** while the chip enable signal $\overline{CE}$ is active low. Addresses and data are latched on the rising edge of the write enable signal $\overline{WE}$.

The flash EEPROM **20** is in the active mode of operation when both control signals $\overline{CE}$ and $\overline{OE}$ are at a logic low level and $\overline{PWD}$ is at a logic high level. When both the chip enable signal $\overline{CE}$ and the power down signal $\overline{PWD}$ are logic high, the flash EEPROM **20** enters the stand-by mode. The power down signal $\overline{PWD}$ causes the flash EEPROM **20** to enter the deep power down mode when the power down signal $\overline{PWD}$ is at a logic low level.

For the active mode of operation, the flash EEPROM **20** may draw sufficient power from the power supply **11** to perform read, program, and erase operations. For the stand-by mode of operation, the flash EEPROM **20** is prevented from performing any operations on the memory cell array **21**, and the amount of power that the flash EEPROM **20** may consume is reduced. For the deep power down mode of operation, all memory cell array operations are disabled and the amount of power that the flash EEPROM **20** may consume is less than that of the stand-by mode. For example, the flash EEPROM **20** may consume 100 microamperes of current while in the stand-by mode and only two microamperes of current while in the deep power down mode. For prior flash EEPROMs that do not include internal power supplies, the deep power down mode results in the disabling of all the circuits of the flash EEPROM.

When the flash EEPROM **20** transitions from either the stand-by mode or the deep power down mode to the active mode, it is desirable for the flash memory cell array **21** be ready to perform for read operations, which means that the wordline switches **23** should be charged to 5.0 volts. If the detected external supply voltage VCC is 5.0 volts, the wordline switches may be maintained at 5.0 volts by the external supply voltage VCC during the stand-by and deep power down modes through the use of a simple pull-up device, which may be a transistor or a resistor. If the detected external supply voltage is VCC 3.3 volts, an internal power supply may be used to charge the wordline switches **23** to 5.0 volts.

If the external supply voltage VCC is equal to 3.3 volts and the internal power supplies are only enabled to charge wordline switches **23** when the flash EEPROM **20** operates in the active mode, the access time for the flash EEPROM **20** is increased when the flash EEPROM transitions from the stand-by or deep power down modes to the active mode to allow the wordline switches **23** to be charged to the appropriate voltage. The wordline switches **23** are discharged due to leakage, and, given sufficient amount of time, the wordlines switches **23** may be discharged to the value of the external supply voltage VCC. Further, wherein the memory cell array **21** is quite large, the capacitance of the wordline switches **23** is increased, which may result in significant voltage and current transients internal to the flash EEPROM **20** when the flash EEPROM **20** transitions between operating modes. Such transients must be accounted for, which typically results in a further increase in access time. Therefore, to decrease the amount of time required to access the flash EEPROM **20** and to reduce internal transients, it may be desirable for the appropriate internal power supply to remain in operation during the stand-by and deep power down modes; however, the design of the smart voltage circuitry may be constrained by the power consumption requirements of the flash EEPROM and by the amount of semiconductor die space that can be provided for the smart voltage circuitry.

FIGS. **3**A and **3**B show the smart voltage circuitry **27** according to two different embodiments. FIG. **3**A shows an example of the smart voltage circuitry **27***a* wherein the wordline switches **23** are maintained at 5.0 volts by the internal power supplies while the flash EEPROM **20** is operating in both the stand-by and deep power down modes. The smart voltage circuitry **27***a* of FIG. **3**A results in a greatly reduced access time, but may require more die space. FIG. **3**B shows an example of the smart voltage circuitry **27***b* wherein the wordline switches **23** are maintained at 5.0 volts by the internal power supplies during the stand-by mode, but are maintained at the external supply voltage VCC during the deep power down mode. The smart voltage circuitry **27***b* of FIG. **3**B typically requires less die space than the circuitry of FIG. **3**A, but access time may be increased.

FIG. **3**A shows smart voltage circuitry **27***a* that includes a VCC ramp detector **30**, a 3.3 v/5 v VCC level detector **35**, a low VCC detector **40**, a current source **45**, a pulse generator **50**, a 5 v/12 v VPP level detector **55**, and internal power supplies **60***a*. The operation of the internal power supplies **60***a* is determined by the mode of operation for flash EEPROM **20**, the external operating supply voltage VCC, and the external programming supply voltage VPP as detected by the VCC ramp detector **30**, the 3.3 v/5 v VCC level detector **35**, and the 5 v/12 v VPP level detector **55**. The

program and erase operations are inhibited if a low external supply voltage VCC level is detected by the low VCC level detector **40** while the flash EEPROM **20** is in the active mode of operation. The current source **45** and the pulse generator **50** are included to conditionally and periodically enable the internal power supplies **60***a* for charging the wordline switches **23** to 5.0 volts while the flash EEPROM operates in either the stand-by or deep power down operating modes. The wordline switches **23** are thus maintained at the requisite voltage level, but the internal power supplies are only periodically activated such that the power consumption of the flash EEPROM **20** may be maintained within the limits defined for the standby and deep power down modes of operation. This circuitry is described in more detail below.

The internal power supplies **60***a* include three output lines. The HH5PX output line may be coupled to the wordline switches **23** for read operations. The HHVPLL output line may be coupled to the bitline switches **25** for programming operations. The HHVP12 output line may be coupled to the wordline switches **23** for programming operations and to the source switches **24** for erase operations.

FIG. **3B** shows smart voltage circuitry **27***b* that typically requires less semiconductor die space than the circuitry shown in FIG. **3A**. Smart voltage circuitry **27***b* includes VCC ramp detector **30**, 3.3 v/5 v VCC level detector **35**, a low VCC detector **40**, 5 v/12 v VPP level detector **55**, and internal power supplies **60***b*, which include a stand-by five-volt internal supply (shown in FIG. **13B**) that is used to charge the wordline switches **23** to 5.0 volts if the external supply voltage VCC is not 5.0 volts, and if the flash EEPROM **20** is operating in the stand-by mode. The stand-by five-volt internal supply is smaller than the five-volt internal supply used during read operations such that power consumption may be maintained within the limits of the stand-by operating mode. The wordline switches **23** are charged to the external supply voltage VCC during deep power down mode, regardless of whether or not external VCC is equal to 5.0 volts. As shown, the same circuitry that is used as a VCC ramp detector **30** may be used as a low VCC detector **40** to further reduce the amount of semiconductor die space required for the smart voltage circuitry **27***b*.

The basic operation of the smart voltage circuitry **27***a* shown in FIG. **3A** will now be discussed. The VCC ramp detector **30** is provided to enable the internal power supplies **60***a* and to initialize the 3.3 v/5 v VCC level detector **35**, the current source **45**, and the pulse generator **50** when power is first applied to the flash EEPROM **20**. The precise operation of VCC ramp detector **30** depends on the mode of operation for the flash EEPROM **20** when power is first applied.

FIG. **23A** shows a method of operation for the smart voltage circuitry **27***a* shown in FIG. **3A** when the flash EEPROM **20** is operating in the deep power down or stand-by modes. At process block **2400**, power is first supplied to the flash EEPROM **20**. At process block **2405**, the VCC ramp detector **30** responds to power-up by enabling the internal power supplies **60***a* to charge the wordline switches **23**, by initializing the 3.3 v/5 v VCC level detector **35** to indicate a 3.3 volt external VCC, and by initializing the current source **45** and the pulse generator **50**.

The VCC ramp detector **30** outputs a control signal HDRMVCD to the 3.3 V/5 V VCC level detector **35**, the current source **45**, the pulse generator **50**, and the internal power supplies **60***a*. When the operating supply voltage VCC is less than a trip-point voltage V_{trip} of the VCC ramp detector **30**, the signal HDRMVCD tracks the external supply voltage VCC as it ramps from zero volts to its final value, and the appropriate circuitry is enabled or disabled.

At process block **2410**, the supply voltage exceeds the trip-point voltage V_{trip}, which may be 2.7 volts or 2.9 volts, and the control signal HDRMVCD goes low. The VCC ramp detector **30** is switched off to reduce the power consumption of smart voltage circuitry **27***a*. In response to the control signal HDRMVCD going low, the 3.3 v/5 v VCC level detector **35** and the internal power supplies **60***a* are disabled, and the pulse generator **50** is enabled. The pulse generator **50** periodically supplies a logic high control pulse to the internal power supplies **60***a* and the 3.3 v/5 v VCC level detector **35** via the HDOUT signal line. The current source **45** is included to provide biasing currents PBIAS and NBIAS to the oscillators (as shown in FIG. **22**) of the pulse generator **50**.

At process block **2415**, a control pulse is received by the internal power supplies **60***a* and the 3.3 v/5 v VCC level detector **35**. The internal power supplies **60***a* are enabled for the duration of each control pulse so that the voltage of the wordline switches **23** may be maintained at 5.0 volts. The 3.3 v/5 v VCC level detector **35**, which is coupled to receive the external supply voltage VCC, is also enabled for the duration of the control pulse. According to one embodiment, a six microsecond pulse is applied once every three milliseconds.

The 3.3 v/5 v VCC level detector **35** outputs a control signal ID5V to indicate the detected value of the external supply voltage VCC. As described above, the control signal ID5V is initialized during power-up of the flash EEPROM **20** to a logic low level for indicating that external VCC is not five volts. If the external supply voltage VCC is greater than a trip-point voltage $V_{3/5}$ for the 3.3 v/5 v VCC level detector **35** while the 3.3 v/5 v VCC level detector **35** enabled, the ID5V signal is set to a logic high level.

At process block **2420**, if the external supply voltage VCC is detected as not being equal to five volts, the internal power supplies **60***a* are allowed to charge the wordline switches **23** at process block **2425**. If the external supply voltage VCC is equal to five volts, the 3.3 v/5 v VCC level detector **35** sets control signal ID5V logic high, which disables the internal power supplies **60***a* and enables external VCC to charge the wordline switches **23** at process block **2430**. The high value of the control signal ID5V is latched. The current control pulse ends at process block **2435**. Process blocks **2415–2435** are repeated for each control pulse received from the pulse generator **50**. If external VCC was detected as being at five volts during a previous control pulse, and external VCC is detected as being 3.3 volts during the current control pulse, the internal charge pumps are enabled at process block **2425**. The process shown in FIG. **23A** may be repeated each time the flash EEPROM **20** is powered up in the stand-by or deep power down modes.

FIG. **23B** shows a method of operation for the smart voltage circuitry **27***a* shown in FIG. **3A** when the flash EEPROM **20** is operating in the active mode. At process block **2450**, power is initially supplied to the flash EEPROM **20**. At process block **2455**, wherein external VCC is less than the trip-point voltage V_{trip} of the VCC ramp detector **30**, the internal power supplies **60***a* are enabled to charge the wordline switches **23**, the 3.3 v/5 v VCC level detector **35** is initialized to indicate a 3.3 volt external VCC, the current source **45** and the pulse generator **50** are initialized, and the low VCC detector **40** and the 5 v/12 v VPP level detector **55** are enabled.

The low VCC detector **40** monitors the VCC supply voltage to detect when the operating supply voltage VCC drops below a trip-point voltage V_{lko} of the low VCC detector **40**. The low VCC detector **40** provides the control signals PDPWR2 and PHLOWVCC to the control engine **26**. If VCC drops below the trip-point voltage V_{lko}, the low VCC detector **40** sets the control signal PHLOWVCC to a logic high level such that the control engine **26** prevents programming and erase operations for the memory cell array **21**. The low VCC detector **40** simultaneously sets the control signal PDPWR2 to a high level to reset the control engine **26**. The low VCC detector **32** may be designed in accordance with the teachings of U.S. Pat. No. 5,301,161, entitled *Circuitry for Power Supply Voltage Detection and System Lockout for a Nonvolatile Memory*, issued of Marc Landgraf et al., and commonly assigned to Intel Corporation of Santa Clara, Calif. Alternatively, as will be described with respect to FIG. **3B**, the VCC ramp detector **30** can be configured to operate as the low VCC detector after power-up of the flash EEPROM **20**.

The 5 v/12 v VPP level detector **55** is coupled to the programming supply voltage VPP for determining whether VPP is 5.0 volts or 12.0 volts. The 5 v/12 v VPP level detector **55** outputs a control signal PD5VPP to the internal power supplies **60***a* and the control engine **26**. The control signal PD5VPP is initially high to indicate a five volt VPP level. The internal power supplies **60** use the control signal PD5VPP to select either the external VPP or the internal supplies during programming and erase operations. The control engine **26** may use the control signal PD5VPP to select the appropriate programming and erase algorithms. The 5 v/12 v VPP level detector **55** may be disabled during stand-by and deep power down to further reduce the power consumption of the smart voltage circuitry **27***a*.

Returning to FIG. **23B**, at process block **2460**, external VCC exceeds the trip-point voltage V_{trip}. All circuits remain enabled, and the pulse generated by the pulse generator is locked out. The remaining process blocks of FIG. **23B** may occur in a different order than shown, depending on the type of access requested while the flash EEPROM **20** is in the active mode.

The 3.3 v/5 v VCC level detector **35** remains enabled after the external voltage VCC exceeds the trip-point voltage V_{trip} of the VCC ramp detector. If the 3.3 v/5 v VCC level detector **35** continues to indicate that external VCC is not equal to five volts at process block **2465**, the internal supplies **60***a* are selected to charge the wordline switches **23** to five volts at process block **2470**. If the 3.3 v/5 v VCC level detector **35** indicates that external VCC is equal to five volts at process block **2465**, the external supply voltage VCC is selected to charge the wordline switches **23** to five volts at process block **2475**.

At process block **2480**, it is determined if the external supply voltage VPP is equal to twelve volts. If external VPP is not twelve volts, the internal power supplies **60***a* are selected to provide the programming and erase voltages at process block **2485**. If external VPP is twelve volts, the external supply voltage VPP is selected to provide the voltages for program and erase operations at process block **2490**. The process ends at process block **2495**. The process of FIG. **23B** may be repeated each time the flash EEPROM **20** is powered up in the active mode.

The operation of the smart voltage circuitry **27***b* shown in FIG. **3B** is now discussed with reference to FIGS. **24A–24B**. FIG. **24A** shows the operation of the smart voltage **27***b* when the flash EEPROM **20** is powered up while operating in the deep power down mode. Power is supplied at process block **2500**. At process block **2505**, the 3.3 v/5 v VCC level detector is initialized to indicate a 3.3 volt external VCC. When external VCC is greater than the trip-point voltage V_{trip} of the VCC ramp detector **30** at process block **2510**, the 3.3 v/5 v VCC level detector is disabled. The wordline switches **23** are charged to the external VCC level. The process ends at process block **2515**.

FIG. **24B** shows a method of operation for the smart voltage circuitry **27***b* shown in FIG. **3B** when the flash EEPROM **20** is operating in the stand-by mode. At process block **2520**, power is first supplied to the flash EEPROM **20**. At process block **2525**, the VCC ramp detector **30** responds to power-up by enabling an internal five-volt power supply (shown in FIG. **13B**) to charge the wordline switches **23** and initializing the 3.3 v/5 v VCC level detector **35** to indicate a 3.3 volt external VCC.

At process block **2530**, the supply voltage exceeds the trip-point voltage V_{trip}. The internal five-volt power supply is disabled, and the internal stand-by power supply is enabled. The 3.3 v/5 v VCC level detector **35** remains enabled. The 3.3 v/5 v VCC level detector **35** continuously monitors external VCC at process block **2535** If external VCC is equal to 5.0 volts, the 3.3 v/5 v VCC level detector **35** sets the control signal ID5V logic high, which disables the internal stand-by power supply such that the wordline switches are charged by the external supply voltage VCC. The operation of the smart voltage circuitry **27***b* when powered up in the active mode is similar to that shown in FIG. **23B**.

The smart voltage circuitry **27** of the flash EEPROM **20** allows the same flash EEPROM **20** to be used in computer systems that provide different operating and programming voltages. The smart voltage circuitry **27** may be adapted to detect and select different supply voltages than those described above; however, the goals of compatibility and versatility should be weighed against the need for low power consumption and the desire for increased density for the memory cell array **21**. Accordingly, each component of smart voltage circuitry **27** should be designed to consume reduced power and to require reduced die space. Some of the components of the smart voltage circuitry **27** will now be discussed in greater detail.

VCC RAMP DETECTOR

The VCC ramp detector **30** will now be discussed in more detail. FIG. **4** shows a latch mode VCC ramp detector **30** that is capable of being in either an "untripped state," wherein the externally provided operating supply voltage VCC is less than the trip-point voltage V_{trip}, or a "tripped state," wherein the external supply voltage VCC is greater than the trip-point voltage V_{trip}. The VCC ramp detector **30** shown in FIG. **4** is said to be a "latch mode" VCC ramp detector because it is disabled once it enters the tripped state. Little or no current is consumed by the latch mode VCC ramp detector **30** while it is in the tripped state. For one embodiment of the flash EEPROM **20**, the latch mode VCC ramp detector **30** is designed to operate only at initial power up of the flash EEPROM **20**. The VCC ramp detector of FIG. **4** may be used in the smart voltage circuitry **27***a* of FIG. **3A**.

The VCC ramp detector **30** is shown as including a flash cell **65**, an n-channel field effect transistor ("FET") **70** having its source coupled to the drain of the flash cell **65**, a p-channel FET **75** having its drain coupled to the drain of FET **70** and its source coupled to external VCC, and an output circuit **85** having its input connected to the node **80** defined by the drain of FET **70** and the drain of FET **75**. The output circuit **85** may include a first inverter **86** having its input connected to node **80** and its output coupled to the input of a second inverter **87**, which outputs the control

signal HDRMVCD. The output of inverter **86** may be fed back to the gate of FET **75**. The inverters **86** and **87** are powered by the input voltage, which, for this example, is the external supply voltage VCC. The latch mode VCC ramp detector **30** also includes a start-up circuit **90** for initially biasing the node **80** and a drain bias control circuit **100** for providing a biasing voltage VDBIAS to FET **70**.

The flash cell **65** is primarily used as a transistor rather than as a memory element. Because the threshold voltage of the flash cell **65** can be varied, the trip-point voltage V_{trip} of the latch mode VCC ramp detector **30** may be varied by programming the flash cell to different V_t levels. The flash cell **65** may alternatively be any type of nonvolatile memory cell, including an EPROM or EEPROM memory cell. Wherein a standard FET may be used in place of the flash cell **65**, the flash cell **65** is advantageous because it may be programmed to account for process variations.

When the computer system **10** is initially switched on, the external supply voltage VCC begins to ramp from zero volts to the final VCC value, which may be either 3.3 volts or 5.0 volts. The start-up circuit **90** is coupled to VCC for initially biasing the node **80** so that the output circuit **85** ramps up with the external supply voltage VCC. For example, the start-up circuit **90** may be configured to output the external VCC until VCC has reached a predetermined voltage level such as 1.5 volts, which causes the output of inverter **86** to go to system ground VSS. The start-up circuit **90** is then switched off and node **80** continues to be pulled up towards the external supply voltage VCC by FET **75**, which is switched on in response to the output of the inverter **86** going to system ground VSS. The control signal HDRMVCD output by the output circuit **85** tracks voltage at node **80**. The latch mode VCC ramp detector **30** enters the untripped state when FET **75** is switched on.

FET **70** is a device that biases the drain of flash cell **65** so that flash cell **65** is prevented from being accidentally programmed. The drain bias control circuit **100** supplies the bias voltage VDBIAS to the gate of FET **70** to bias FET **70** such that the drain of flash cell **65** does not exceed 1.5 volts. Wherein another type of nonvolatile memory cell is used in place of the flash cell **65**, FET **70** may not be required.

As shown, the external operating supply voltage VCC is applied to the gate of flash cell **65**, which is programmed to have a threshold voltage V_t that sets the trip-point voltage V_{trip} of the latch mode VCC ramp detector circuit **30** to the desired value. According to one embodiment, the trip-point voltage V_{trip} is equal to 2.9 volts. Typically, the threshold voltage V_t of the flash cell is programmed such that the voltage at node **80** is detected as a logic low when the external supply voltage exceeds the trip-point voltage V_{trip}. Because the flash cell **65** is programmable, process variations in the devices of the latch mode VCC ramp detector **30** may be accounted for by programming the V_t of flash cell **65**. Flash cell **65** may be programmed by applying the appropriate voltages to flash cell, as shown in FIG. **2**.

When the gate-to-source voltage V_{gs} of the flash cell **65**, which is equal to VCC-VSS, exceeds the threshold voltage Vt of the flash cell **65**, the flash cell **65** turns on such that a drain-source current I_{ds} flows through the flash cell **65**, pulling the node **80** down towards system ground VSS. When the voltage at node **80** is pulled sufficiently low, the inverter **86** outputs the current value of the external supply voltage VCC, which switches FET **75** off so that no DC current flows from VCC to ground. The control signal HDRMVCD is set to system ground VSS. The latch mode VCC ramp detector **30** enters the tripped state when the FET **75** is switched off, and the latch mode VCC ramp detector **30** will not return to the untripped state until external VCC goes to zero or the VCC ramp detector **30** is reset by external logic.

FIG. **5** shows waveforms that describe the operation of the VCC ramp detector shown in FIG. **4**. Waveform **91** shows the behavior of the external operating supply voltage VCC; waveform **92** shows the voltage of the node **80**; waveform **93** shows the voltage at node **88**, which is defined between inverters **86** and **87**; and waveform **94** shows the voltage at the output of the VCC ramp detector **30**. As shown, the output of the output circuit **85** tracks the external supply voltage VCC until VCC reaches the trip-point voltage V_{trip}, at which time the output of output circuit **85** is pulled down to system ground VSS. The output circuit **85** may alternatively include only the inverter **86** such that the output signal HDRMVCD is shown by waveform **93**.

The VCC ramp detector shown in FIG. **4** may be altered to act as a general purpose voltage detector that continuously monitors the value of the externally provided operating supply voltage VCC. A VCC ramp detector that operates in this manner is called a "continuous mode" voltage detector. A continuous mode voltage detector may freely pass between the tripped and untripped states in response to the input voltage.

FIG. **6** shows a continuous mode voltage detector **96**. The continuous mode voltage detector **96**, like the latch mode VCC ramp detector, includes flash cell **65**, FET **70**, FET **75**, output circuit **85**, and drain bias control circuit **100**. The start-up circuit **45** is not required because a bias signal VCBIAS is applied to the gate of the p-channel FET **75** by the current bias circuit **95** so that the node **80** is pulled towards the supply voltage VCC via the drain-source current of FET **75**. To reduce the current consumed by the continuous mode VCC ramp detector, the bias signal VCBIAS supplied by the current bias circuit **95** biases FET **75** to be a weak pull-up device. The bias signal VCBIAS is such that the current sourced by FET **75** is independent from the value of the external operating supply voltage VCC.

The control signal HDRMVCD supplied by the output circuit **85** tracks the voltage of node **80**. When the external supply voltage VCC is less than the threshold voltage V_t of the flash cell **65**, the voltage at node **80** ramps up with the external supply voltage VCC. When the external supply voltage VCC exceeds the threshold voltage V_t of the flash cell **65**, the flash cell **65** is switched on such that the voltage at node **80** is pulled towards ground and the output circuit **85** sets the control signal HDRMVCD to a logic low level. Should the external supply voltage VCC drop below the threshold voltage of the flash cell **65**, the continuous mode VCC ramp detector **30** reenters the untripped state, and HDRMVCD is set to the present level of the external supply voltage VCC. The continuous mode VCC ramp detector may therefore be used as a low VCC detector.

FIG. **7** shows waveforms that describe the behavior of the continuous mode voltage detector. Waveform **101** shows the behavior of the external operating supply voltage VCC; waveform **102** shows the voltage at node **80** in response to the supply voltage VCC; waveform **103** shows the voltage at node **88**; and waveform **104** shows the signal HDRMVCD output by the continuous mode VCC ramp detector **30**. Waveforms **102** and **104** show that the continuous mode voltage detector **96** detects when the operating supply voltage VCC falls below the trip point voltage V_{trip} so that the voltage detector may be used as a low VCC detector circuit or as VCC or VPP level detector circuit. The output circuit **85** may alternatively include only the inverter **86** such that the output signal HDRMVCD is shown by waveform **103**.

FIG. 8 shows a switchable mode voltage detector 109 that can operate in the latch mode and the continuous mode. According to one embodiment, the switchable mode voltage detector 109 operates as the latch mode VCC ramp detector 30 at power-up and in the deep power down mode. The switchable mode voltage detector 109 operates in the continuous mode as the low VCC detector 40 after power-up while the flash EEPROM 20 operates in the stand-by and active modes. The switchable mode voltage detector 109 includes flash cell 65, FET 70, FET 75, output circuit 85, start-up circuit 90, current bias circuit 95, drain bias circuit 100, p-channel FET 105, and feedback control circuit 110. The p-channel FET 105 has its drain coupled to the source of FET 75, its source coupled to the operating supply voltage VCC, and its gate coupled in a feedback configuration with the output circuit 85 via feedback control circuit 110.

When the flash EEPROM is initially powered-up, the feedback control circuit 110 couples the output of the inverter 86 (as shown in FIG. 6) to the gate of FET 105, and the start-up circuit 90 biases node 80 so that the output of inverter 86 goes low, switching FET 105 on. The switchable mode voltage detector 109 therefore initially operates in the latch mode. Once the value of the operating supply voltage VCC exceeds the threshold voltage V_t of flash cell 65, the VCC ramp detector 30 is placed in the tripped state where it remains until the flash EEPROM enters the stand-by or active modes. When the flash EEPROM 20 enters the stand-by or active modes, the feedback control circuit decouples the output of the output circuit 85 from the gate of the FET 105 and instead supplies a biasing voltage to the gate of FET 105 so that FET 105 is switched on. The VCC ramp detector 30 is therefore in the continuous mode and may be configured to act as the low VCC detector 40.

As described above, the flash EEPROM 20 is capable of operating in the stand-by and deep power down modes, as well as in the active mode. For the stand-by and deep power down modes, it is important to reduce the power consumption of the continuous mode and switchable mode voltage detectors so that the overall power consumption of the flash EEPROM 20 remains within defined limits. One way to reduce power consumption during the stand-by mode is to bias FET 75 to act as a weak pull-up device having a high impedance such that current flow is reduced. For the deep power down mode, the power consumption of the continuous mode voltage detector 96 can be reduced to zero by switching off FET 75. The switchable mode voltage detector 109 may switch off both FET 75 and FET 105 during the deep power down mode to reduce power consumption.

FIG. 9 shows a drain bias control circuit in more detail. As shown, the biasing voltage VDBIAS is derived from the operating supply voltage VCC to control the drain voltage V_{drain} at the drain of the flash cell 65. The drain voltage V_{drain} of the flash cell 65 may be expressed by the following equation:

$$V_{drain}=VDBIAS-V_{t70},$$

wherein V_{t70} is the threshold voltage of FET 70. The biasing voltage VDBIAS is equal to VCC minus any diode drops associated with diode connected FETs 115 and 120 that may be inserted between the operating supply voltage VCC and the output of the drain bias control circuit 100.

According to one embodiment, the value of VDBIAS is selected such that the maximum drain voltage V_{drain} is less than 1.5 volts, regardless of the value of the trip-point voltage V_{trip}. Once flash cell 65 switches on, which occurs when the external supply voltage VCC exceeds the trip-point voltage of the VCC ramp detector 30, the drain voltage V_{drain} is pulled to ground. Therefore, the maximum drain voltage occurs when VCC is equal to the trip-point voltage V_{trip}. As the trip-point voltage increases, more diode-connected FETs may be connected in series as shown in FIG. 9 to reduce the value of VDBIAS such that the drain voltage V_{drain} does not exceed the predefined maximum drain voltage.

FIG. 10 shows a continuous mode clocked voltage detector circuit 121 that operates similarly to the voltage detector circuits shown in FIGS. 4, 6, and 8. The clocked voltage detector circuit 121 may be altered to be operate in both the continuous mode and the latch mode as shown in FIG. 8. The design of the clocked voltage detector circuit 121 reflects the fact that supply voltage levels typically do not change that rapidly. Therefore, the clocked voltage detector circuit 121 is designed to detect the values of both the operating supply voltage VCC and the programming supply voltage VPP at different times. The clocked voltage detector circuit 121 includes flash cells 125 and 130, one of which is selected by the multiplexor 135 to define the trip-point voltage V_{trip} of the clocked voltage detector circuit 121 in response to the control signal CTL, which may be provided by the control engine 26. The threshold voltage of flash cell 125 may be programmed such that the clocked voltage detector circuit 121 operates as the 3 v/5 v VCC level detector when flash cell 125 is selected. Similarly, the threshold voltage of flash cell 130 may be programmed such that the clocked voltage detector circuit 121 operates as the 5 v/12 v VPP level detector when flash cell 130 is selected. More flash cells may be added so that the clocked voltage detector may also operate as the VCC ramp detector circuit and the low VCC level detector circuit. The power supply of the NAND gate 145 may be multiplexed to be either VCC or VPP.

A switch circuit 140 is coupled to the external supply voltages VCC and VPP. The switch circuit 140 may include a resistive divider circuit (not shown) to reduce the external programming supply voltage VPP to a lower level. The control signal CTL selects one of the supply voltages to be provided to the gates of the flash cells 125 and 130. The clocked voltage detector circuit 121 is clocked by a CLK signal. For the output circuit 85, the clocked voltage detector 121 includes a two-input NAND gate 145 having one input coupled to node 80 and the other input coupled to the CLK signal. When the CLK signal is low, the output of the NAND gate 145 is logic high. When the CLK signal goes high, the output of the NAND gate 145 is determined by the voltage at node 80. If the selected supply voltage is greater than the threshold voltage of the selected flash cell, the voltage at node 80 is set to system ground VSS and the NAND gate 145 outputs a logic high voltage. Otherwise, the voltage at node 80 is high such that the NAND gate 145 outputs a logic low voltage. One or more latches (not shown) may be coupled to the output of the clocked voltage detector circuit and controlled by the CLK and CTL circuits to latch the output of the clocked voltage detector circuit 121 at the appropriate times. These latched values may be provided to the control engine 26.

5 V/12 V VPP DETECTOR

The 5 v/12 v VPP level detector 55 detects whether the programming supply voltage VPP is equal to 5 volts or 12 volts. FIG. 11 shows the 5 v/12 v VPP level detector 55 according to one embodiment. The 5 v/12 v VPP level detector 55 includes p-channel FETs 150–153 and 155, n-channel FETs 170 and 175, resistor 160, and inverter 165. The source of FET 150 is coupled to the external supply voltage VPP, and the drain of FET 150 is coupled to the

source of FET **151**. The drain of FET **151** is coupled to the source of FET **152**, which has its drain coupled to the source of FET **153**. The drain of FET **153** is coupled to system ground VSS. Each of the FETs **150–153** have their gates coupled to their drains.

The voltage at the node between the drain of FET **150** and the source of FET **151** is coupled to the gate of FET **155**. The source of FET **155** is coupled to the external programming supply voltage VPP, and the drain of FET **155** is coupled to a node **157**. The resistor **160** is coupled between node **157** and system ground VSS. The inverter **165** has its input coupled to the node **157** for detecting the voltage at node **157**. The inverter **165** is powered on the low side by system ground VSS and on the high side by the voltage at node **167**, which is determined by the n-channel FETs **170** and **175**.

The gate and drain of FET **170** are coupled to the programming supply voltage VPP, and the gate and drain of FET **175** are coupled to the external operating supply voltage VCC. The n-channel FET **175** is shown as a "K device" that has a low threshold voltage and that can operate at high voltages. The FETs **170** and **175** are provided to better ensure correct operation of the 5 v/12 v VPP level detector **55** for the case wherein the operating supply voltage VCC is greater than the programming supply voltage VPP.

The operation of the circuit shown in FIG. **11** will now be discussed with respect to the time when power is first supplied to the flash EEPROM **20**, at which time the external programming supply voltage VPP is equal to zero volts and begins to ramp towards its final value, which may be 5.0 volts or 12 volts. Initially, the voltage at node **157** is at system ground VSS, and the inverter **165** sets the control signal PD5VPP at a logic high level. As the programming supply voltage VPP increases, the amount of drain-source current for FET **155** increases, and node **157** begins to be pulled up towards the final value of VPP. If external VPP is sufficiently high, FET **155** acts as a strong pull-up device that overcomes the pull-down resistor **160**. The inverter **165** sets the control signal PD5VPP at a logic low level if the voltage at node **157** is detected to be at a logic high level, indicating that the external programming supply voltage VPP is 12 volts.

Wherein the circuit shown in FIG. **11** is sufficient for detecting the value of the programming supply voltage VPP, improvements may be made. For example, if the operating supply voltage VCC is greater than the programming supply voltage VPP, the circuit shown in FIG. **11** draws a constant DC current. Further, the resistor **160** occupies a relatively large amount of semiconductor die space, which may affect the density of the memory cell array **21**.

FIG. **12** shows the 5 v/12 v VPP level detector **55** according to a second embodiment. To reduce the amount of semiconductor die space required for the 5 v/12 v VPP level detector **55**, the resistor **160** has been replaced with n-channel transistors **185** and **190**, which present an active load to the drain of FET **155**. The 5 v/12 v VPP level detector of FIG. **12** is shown as including p-channel FETs **150–153**, **155**, **180**, **200**, and **215**; n-channel FETs **185**, **190**, **195**, **205**, and **210**; and inverters **220** and **225**.

The FETs **150–153** are coupled as described above with respect to FIG. **11**, and the gate of FET **155** is coupled to receive the voltage from the node **156** defined between the drain of FET **150** and the source of FET **151**. The source of FET **155** is coupled to the programming supply voltage VPP, and the drain of FET **155** is coupled to the drain of FET **185**, which is a K device. FET **185** is provided to isolate FET **190** from the high voltages that may arise at node **191**, and FET **185** may not be required if the voltage detector circuit shown in FIG. **12** is used to detect lower voltages, which may occur if the circuit were adapted to be a 3.3 v/5 v VCC level detector. The gate of FET **185** is coupled to receive the voltage from the node **157** defined between the drain of FET **151** and the source of FET **152**, and the source of FET **185** is coupled to the drain of FET **190**. FET **190** has its source coupled to system ground VSS and its gate coupled to the node **158** defined between the drain of FET **152** and the source of FET **153**.

A node **191** is defined between the drain of FET **155** and the drain of **185**. The voltage at node **191** drives the gates of p-channel FET **200** and n-channel FET **205**, which are coupled to operate as an inverter. The source of FET **200** is coupled to the operating supply voltage VCC, and the drain of FET **200** is coupled to the drain of FET **205**. The node **192** defined between the drain of FET **200** and the drain of FET **205** determines the value of the control signal PD5VPP output by the 5 v/12 v VPP level detector **55**. The inverter **220** has its input coupled to node **192** and its output coupled to the input of inverter **225**, which outputs the control signal PD5VPP. The FET **215** has its gate coupled to the programming supply voltage VPP, its source coupled to the operating supply voltage VCC, and its drain coupled to the node **192**. FET **195** has its gate coupled to node **158** and its source coupled to the drain of FET **210**, which has its source coupled to system ground VSS and its gate coupled to the programming supply voltage VPP. FET **195** is selected to have the same characteristics as FET **190**.

FETs **150–153** may be identical devices each having a channel width of five microns and a channel length of twenty microns. FETs **150–153** act as a voltage divider and provide voltages to the gates of FETs **155** and **190** such that the absolute value of the gate-to-source voltages V_{GS} for both FET **155** and FET **190** are equal. For example, the gate voltage for FET **155** is equal to three-fourths VPP such that V_{GS155} is equal to negative one-fourth VPP, and the gate voltage for FET **190** is equal to one-fourth VPP such that V_{GS190} is equal to one-fourth VPP. FETs **190** and **195** are also identical devices having a channel width of two microns and a channel length of thirty microns. FET **155** may actually be four identical FETs coupled in parallel, each having a channel width of five microns and a channel length of twenty microns. Example threshold voltages for FETs **155**, **185**, **190**, and **195** are 1.5 volts for FET **155**, 0.2 volts for FET **185**, and 1.0 volt for FETs **190** and **195**.

FET **155** essentially acts as a pull-up device for node **191**, and FET **190** essentially acts as a pull-down device for node **191**. The trip-point voltage $V_{5/12}$ for the 5 v/12 v VPP level detector **55** occurs when the voltage at node **191** is approximately equal to one-half VCC. When node **191** is charged to the trip-point voltage $V_{5/12}$, both FETs **155** and **190** are saturated, and the gate-source voltages and the drain-source currents of FETs **155** and **190** are approximately equal. The trip-point voltage $V_{5/12}$ may approximated using the following equation:

$$V_{5/12} = c\left(\frac{\sqrt{\beta_{155}}\ V_{T155} - \sqrt{\beta_{190}}\ V_{T190}}{\sqrt{\beta_{155}} - \sqrt{\beta_{190}}}\right),$$

wherein c is a constant determined by the common gate-source voltage applied to FETs **155** and **190**; V_{T155} is the threshold voltage for FET **155**; V_{T190} is the threshold voltage for FET **190**; β_{155} is the beta value for FET **155**; and β190 iS the beta value for FET **190**. For the circuit shown in FIG. **12**, c is equal to four.

The beta values for FETs **155** and **190** may be expressed by the following equations:

$$\beta_{155} = k_{155}\frac{w_{155}}{l_{155}},$$

and

$$\beta_{190} = k_{190}\frac{w_{190}}{l_{190}},$$

wherein w_{155} is the channel width for FET **155**, l_{155} is the channel length for FET **155**, w_{190} is the channel width for FET **190**, and l_{190} is the channel length for FET **190**. The trip-point voltage $V_{5/12}$ may be set by varying the threshold voltages and beta values of the FETs **155** and **190**, and by changing the gate-source voltage applied to FETs **155** and **190**.

A number of the devices shown in FIG. **12** are provided to protect against the occurrence of certain conditions for the circuit. For example, it is undesirable for node **192** to float at an intermediate voltage because inverter **220** may respond to such an intermediate voltage by drawing DC current. Thus, FETs **215** and **180** are provided to better ensure that node **192** is set at either a high or a low logic level. FET **215** sets node **192** to VCC if VPP is less than VCC by the threshold voltage of FET **215**. FET **180** is provided to set node **156** to VPP when the supply voltage VPP is at a relatively low voltage. This results in the gate source voltage of FETs **190** and **195** being set to one-third VPP such that FETs **190** and **195** are switched on earlier. Node **191** is therefore set to system ground, and node **192** is set to VCC. FET **180** thus guards against the case wherein VCC and VPP are approximately the same voltage such that FET **215** does not switch on. When VPP is increased, FET **180** is essentially an open circuit such that all current flows through the voltaged divider circuit and node **156** is set to three-fourths VPP.

During normal operation, once the programming supply voltage VPP has increased enough such that the voltage at node **158** exceeds the threshold voltage of FET **190** and **195**, FETs **190** and **195** are switched on. As described above, the FETs **190** and **195** are matched such that they have the same threshold voltage. Node **193** is no longer floating, and FET **185** is switched on. When first switched on, FETs **190** and **185** are operating in the linear region and appear as a low resistance load to FET **155**, and the voltage at node **191** is pulled down to system ground VSS. As VPP continues to increase, the gate-source voltage of FET **185** increases, the drain-source current of FET **155** increases, and the equivalent resistance presented to the source of FET **155** by the FETs **185** and **190** increases.

If the programming supply voltage VPP rises beyond 5.0 volts, the trip-point voltage of the 5 v/12 v VPP level detector **55** is approached. When the programming supply voltage VPP is equal to the trip-point voltage $V_{5/12}$ of the 5 v/12 v VPP level detector **55**, the equivalent resistance of the FETs **185** and **190** and the drain-source current of the FET **155** have increased such that the node **191** begins to be pulled up to the programming supply voltage VPP. When the voltage at node **191** is greater than the threshold voltage of FET **205**, the voltage at node **192** pulled down to system ground VSS, which causes the control signal PD5VPP to be set at a logic low level.

The equivalent resistance of the FETs **185** and **190** is very high, much higher than the resistance that typically can be achieved with a resistor using the same amount of semiconductor die space. As the resistance presented by FETs **185** and **190** is higher than the resistance of the resistor **160** used in the circuit of FIG. **11**, the amount of current required by the circuit of FIG. **12** is reduced when compared to the current consumption of the circuit of FIG. **11**. The gain of the circuit is increased such that voltage at node **192** can swing between VSS and VPP much more quickly than the circuit shown in FIG. **11**.

Internal power supplies

FIG. **13***a* and **13***b* show the internal power supplies **60** according to different embodiments. The internal power supplies **60***a* shown in FIG. **13**A may be those for the smart voltage circuitry **27***a* shown in FIG. **3**A. The internal power supplies **60***b* shown in FIG. **13**B may be those for the smart voltage circuitry **27***b* shown in FIG. **3**B.

As shown in FIG. **13**A, the internal power supplies **60***a* may generally include a five volt internal supply **240**, a nine volt internal supply **245**, and a twelve volt internal supply **250**. The internal supplies **240–250** may be enabled to generate the higher voltages required to perform operations on the memory cell array if the external supply voltage levels are too low. The 5 v internal supply **240** is shown as being coupled to receive the control pulse from the pulse generator via the HDOUT signal line so that the wordline switches **23** may be charged to the correct voltage while the flash EEPROM **20** is operating in the stand-by or deep power down modes.

Also included are a plurality of switches **255–280** that are controlled by the control logic **230** to select either the supply voltages or the outputs of the appropriate internal power supplies in response to the detected voltages, the operating mode of the flash EEPROM **20**, and the particular operation to be performed. A switch is provided on each side of an internal supply such that the internal supply may be isolated from the remaining circuitry when the internal supply is not selected to provide power to the memory cell array **21**. For example, switch **270** is opened and switch **255** selects the external VCC supply pin when external VCC is equal to five volts. Similarly, switches **275** and **280** are open, and switches **260** and **265** select the external VPP supply pin when external VPP is equal to twelve volts. FIG. **13**A shows a case wherein external VCC is 3.3 volts, and external VPP is five volts. The use of switches in this manner reduces the amount of current consumed by the internal power supplies **60**.

The control logic **230** receives the control signals ID5V and PD5VPP for detecting the values of the operating supply voltage VCC and the programming supply voltage VPP. The control logic **230** is coupled to receive the control signals $\overline{CE}$ and $\overline{PWD}$ for detecting the mode of operation of the flash EEPROM **20**. The control logic **230** is also coupled to receive the control signal HDOUT output by the pulse generator **50**. When the flash EEPROM is in the stand-by or deep power down modes, the five volt internal supply **240** is periodically switched on in response to the control signal HDOUT output by the pulse generator **50**.

Referring now to FIG. **13**B, the internal power supplies **60***b* may generally include a stand-by five volt internal supply **235**, a five volt internal supply **240**, a nine volt internal supply **245**, and a twelve volt internal supply **250**. Also included are a plurality of switches **255–285** that are controlled by the control logic **230** to select either the supply voltages or the outputs of the appropriate internal power supplies in response to the detected voltages, the operating mode of the flash EEPROM **20**, and the particular operation to be performed. A switch **285** is provided between the external VCC supply pin and the stand-by internal supply **235**.

The control logic **230** receives the control signals ID5V and PD5VPP for detecting the values of the operating supply voltage VCC and the programming supply voltage VPP. The control logic **230** is coupled to receive the control signals $\overline{CE}$ and $\overline{PWD}$ for detecting the mode of operation of the flash EEPROM **20**. When the flash EEPROM is in the stand-by mode, the stand-by five volt internal supply **235** is enabled to charge the wordline switches to five volts if external VCC is 3.3 volts.

Wherein the internal power supplies **60***a* and **60***b* shown in FIGS. **13**A and **13**B are sufficient, four separate internal supply circuits require large amounts of semiconductor die space. FIG. **14** shows a general internal supply circuit **310** that includes regulation circuitry **315** and a bootstrap charge pump **320**. The charge pump **320** is a typically two-stage or a three-stage circuit, but may alternatively include as many stages as required to provide the desired output voltage.

As shown, the regulation circuit **315** includes a voltage reference circuit **316**, a divider circuit **317** and a voltage-controlled oscillator ("VCO") **318**. The voltage reference **316** is coupled to the input voltage V_{in}, which may be the operating supply voltage VCC or the programming supply voltage VPP. The voltage reference **316** uses the input voltage V_{in} to generate a reference voltage V_{ref} that is supplied to the positive terminal of VCO **318**. The negative terminal of VCO **318** is coupled to the output of the internal supply **310** via the divider circuit **317**. The VCO **318** compares the reference voltage V_{ref} to the output of the divider circuit **317** and outputs a regulation signal REG to the charge pump **320**.

FIG. **15** shows a charge pump **320** in more detail. Charge pump **320** is shown as a three-stage charge pump that includes an oscillator **323** coupled to receive the regulation signal REG, a first phase (PH1) clock driver circuit **325**, a second phase (PH2) clock driver circuit **330**, and a boost circuit **332**. The PH1 and PH2 clock driver circuits are coupled to receive a clock signal output by oscillator **323** in response to the regulation signal REG, wherein the PH1 and PH2 clock driver circuits supply different phases of the clock signal to the boost circuit **332**. The boost circuit **332** generally comprises the switches and capacitors necessary to boost the input voltage to the desired output voltage. The charging and discharging of the capacitors is controlled by the PH1 and PH2 clock driver circuits. An SBREG signal input is provided between the oscillator **323** and the clock drivers **325** and **330** for receiving a clock signal directly from the stand-by regulation circuitry described in FIG. **19**. For alternative embodiments, each of the regulation circuits may include their own clock driver circuits that are multiplexed to control the boost circuit **332**.

The boost circuit **332** includes a number of stages of n-channel FETs **340**, **360**, **380**, and **395** connected in series between the input supply V_{in} and the output terminal V_{out}. The FETs **340**, **360**, and **380** are used to switch current from one stage to the next and are therefore called "switching FETs." The two-stage bootstrap charge pump **320** also includes FETs **335**, **355**, and **375**, which are used to control the operation of the switching FETs and are therefore called "control FETs." All of the FETs may be a type of n-channel FET referred to as an "S type device." S type devices are n-channel FETs having a very low threshold voltage level. The use and manufacture of S type devices are described in detail in U.S. Pat. Nos. 4,052,229; 4,096,584; 4,103,189; and 5,057,715.

The clock phase PH1 is provided to the three-stage bootstrap charge pump **320** via capacitors **345**, **370**, and **385**. Switching FETs **340** and **380** and control FET **355** are switched on and off in response to the PH1 clock signal. The clock phase PH2 is provided to the boost circuit **332** via capacitors **350**, **365**, and **390**. Switching FET **360** and control FETs **335** and **375** are switched on and off in response to the PH2 clock signal. The switching FET **395** has its gate coupled to its drain such that it is typically switched on at all times.

Referring to FIG. **16**, the two clock phases PH1 and PH2 do not overlap, and the PH2 clock signal is shown as being initially high. When the PH2 clock signal is high, switching FET **360** and control FETs **335** and **375** are all switched on. Initially, the drain and gate of the switching FET **360** are at the same voltage. Because the PH1 clock signal is low, the control FET **355** joining the drain of the switching FET **360** to the gate of switching FET **360** is switched off, and current flows through the switching FET **360**. This current transfers charge from the capacitor **350** to the capacitor **370**, reducing the drain voltage of the FET **360** such that the switching FET **360** switches completely on, increasing the current furnished to the next stage.

As the voltages at the drain and source of the switching FET **360** begin to equalize, the voltage at the gate of the control FET **355** is raised so the control FET **355** is nearly on. When the PH2 clock signal goes low, the control FET **355** turns on, and the switching FET **360** begins to turn off. Simultaneously, the control FETs **335** and **375** are turned off such that the gate of FET **340** is isolated from the drain of FET **340**, and the gate of FET **380** is isolated from the drain of FET **380**. When the PH1 clock signal goes high, the control FET **355** switches completely on, equalizing the voltages at the gate and drain of the switching FET **360**. Switching FETs **340** and **380** are switched on response to the PH1 clock signal going high.

The switching FETs **340** and **380** function similarly to the switching FET **360** to transfer charge to the capacitors **350** and **390**, respectively. Thus, when the PH1 clock signal goes high, the switching FET **340** is switched on and current provided by the input supply V_{in} charges the capacitor **350**. Similarly, the switching FET **380** switches on and current provided by the capacitor **370** charges the capacitor **390**. The capacitor **350** tends to be charged to twice the input supply voltage V_{in}, wherein the capacitor **370** tends to be charged to three times the input supply voltage V_{in}, and the capacitor **390** tends to be charged to four times the input supply voltage V_{in}. The boost capacitor voltages are provided by the PH1 and PH2 clock signals, which operate to charge the capacitors further. For example, the capacitor **370** is charged to twice V_{in} by the capacitor **350** and to three times V_{in} by the PH1 clock pulse. The maximum output voltage V_{out} of the charge pump **320** is thus approximately equal to the four time the input supply voltage V_{in} less the threshold voltage of the output FET **395**. The output voltage V_{out} can be controlled by varying the pulse widths of the clock signals.

The capacitors of the boost circuit **332** and the oscillator **323** typically require large amounts of semiconductor die area, and each internal supply of FIG. **13** includes its own charge pump having an oscillator and boost circuit. Substantially identical circuitry may be used for each charge pump because the circuitry of the charge pump can typically be used for any input supply voltage V_{in}. Therefore, to reduce the semiconductor die space required for the internal power supplies **60**, the same charge pump can be used for multiple internal power supplies, wherein the appropriate regulation circuitry is multiplexed to control the output voltage of the common charge pump **320**.

FIG. **17** shows the internal power supplies **60** wherein a common charge pump **320***a* is shared by the stand-by five volt internal supply, the five volt internal supply, and the nine volt internal supply. The twelve volt internal supply is shown as including a separate charge pump **320***b*. A multiplexor **416** has a first input coupled to the output of the five

volt regulation circuitry **405** and a second input coupled to the output of the nine volt regulation circuitry **410**. The output of the multiplexor **416** is coupled to the input of the oscillator for the charge pump **320***a*. A separate switch **418** is provided between the stand-by regulation circuitry **400** and the clock drivers of the charge pump **320***a* such that the oscillator of the charge pump **320***b* is bypassed when the charge pump **320***a* is used as part of the stand-by five volt internal supply **235**.

The control logic **230** is coupled to control the multiplexor **416** and the switch **418**, and the control logic **230** determines which of the stand-by regulation circuitry **400**, the five volt regulation circuitry **405**, and the nine volt regulation circuitry is coupled to the charge pump circuit **320***a* in response to the operating mode of the flash EEPROM **20** and the current operation being performed on the memory cell array **21**. The switches **255–285** are operated as discussed above. Switch **419** is provided to supply either external VCC or VPP to the charge pump **320***a*. Charge pump **320***b* is supplied with external VPP.

Further reduction of the size of the internal power supplies **60** may be achieved by recognizing that a large charge pump is not required to supply twelve volts during programming. Thus, as shown in FIG. **18**, a small twelve-volt programming charge pump **416** may be used during programming operations, such that a single charge pump circuit **320** may be shared to generate the five volt read voltage, the nine volt program voltage, and the twelve volt erase voltage. This reduces the overall size of the internal power supply circuits. An additional switch **417** is provided between the output of the program charge pump **416** and HHVP12. For this embodiment, the multiplexor includes a third input coupled to the output of the twelve volt regulation circuitry **415**.

Stand-by Regulation Circuitry

FIG. **19** shows stand-by regulation circuitry **400** for controlling the five volt charge pump during stand-by and deep power down modes. As described above with respect of FIG. **3B**, if the operating supply voltage VCC is 3.3 volts and the flash EEPROM **20** is in the stand-by operating modes, the stand-by five-volt internal supply is enabled to maintain the voltage of the wordline switches at 5 volts.

The stand-by regulation circuitry **400** includes a transconductance operational amplifier **420**, proportional voltage generator **430**, a voltage reference **435**, and a current controlled oscillator **425**. The operational amplifier **420** outputs a current I_{out} that is proportional to the difference in voltages detected at the positive and negative input terminals. The current controlled oscillator outputs the SBREG signal in response to the current I_{out}, and SBREG is drives the clock drivers of the charge pump **320**.

The positive input terminal of op-amp **420** is coupled to the output of the voltage reference circuit **435**, which may be manufactured according to the teachings of U.S. Pat. No. 5,339,272, entitled *Precision Voltage Reference,* issued of Kerry Tedrow et al., and commonly assigned to Intel Corporation of Santa Clara, Calif. The negative input terminal of op-amp **420** is coupled to the output of a proportional voltage generator **430** having its input coupled to the output of the charge pump **320**, which is coupled to the wordline switches **23**. The op-amp **420** compares the voltages at its terminals and outputs a current I_{out} in response to the comparison, and the current controlled oscillator **425** varies the frequency of SBREG in response to the amount of current I_{out} received from the operational amplifier **420**.

The Pulse Generator

As described above with respect to FIG. **3A**, the internal power supplies **60***a* of smart voltage circuitry **27***a* are periodically enabled to charge the wordline switches **23** to five volts when the flash EEPROM **20** is not in the active mode and external VCC is 3.3 volts. FIG. **20** shows the output of the pulse generator **50** as a function of time. As described above, the five-volt internal power supply is enabled for a single pulse of duration t_p once every t_{total} seconds. A current I_{charge} is consumed by the five volt internal supply for the duration of a pulse, after which the current I_{charge} falls to zero. The amount of current I_{charge} consumed at any given pulse is determined by the amount of charging required to charge the wordline switches **23** back up to 5.0 volts. The time t_{total} is chosen in view of the RC time constant for the wordline switches **23**, the maximum allowable voltage drop on the wordline switches **23**, and a worst case leakage current for the memory cell array **21**. The time t_p is chosen in view of the RC time constant for the wordline switches **23** and the amount of current that the five-volt internal power supply can source. The pulse generator is designed to supply a pulse having the duration t_p once every t_{total} seconds.

Because the pulse generator **50** is designed to operate when the flash EEPROM **20** is in either the stand-by or deep power down modes of operation, the pulse generator **50** should consume as little current as possible so that the power consumption of the flash EEPROM **20** does not exceed the maximum power consumption for the stand-by and deep power down modes. FIG. **21** shows the pulse generator **50** in block diagram form. The pulse generator **50** generally includes a low frequency oscillator circuit **450** and a high frequency oscillator circuit **455**. Both the low frequency oscillator circuit **450** and the high frequency oscillator circuit **455** are coupled to receive the biasing signals PBIAS and NBIAS from the current source circuit **45**. For one embodiment, PBIAS and NBIAS each provide 40 nanoamperes of current.

The high frequency oscillator **455** is coupled to receive the output signal of the low frequency oscillator circuit **450**. The high frequency oscillator **455** is also feedback connected to its own output such that the high frequency oscillator **455** outputs a pulse having the duration of one-half the period for the high frequency oscillator **455** once every period for the low frequency oscillator **450**. For example, wherein the period of the low frequency oscillator **450** is equal to three milliseconds and the period of the high frequency oscillator **455** is equal to twelve microseconds, the high frequency oscillator **455** outputs a pulse having a six microsecond duration once every three milliseconds.

FIG. **22** shows the low frequency oscillator circuit **450** in more detail. The low frequency oscillator circuit **450** is shown as a ring oscillator circuit comprising an odd number of inverters **460–510** coupled in a feedback configuration. Specifically, inverters **460–510** are coupled in series, and the output of inverter **510** is fed back as the input of inverter **460**. There may be more or less inverters, depending on the desired frequency of oscillation.

The output of the low frequency oscillator circuit **450** is the output of the inverter **485**. The positive rail of each inverter is coupled to the operating supply voltage VCC via a corresponding pair of p-channel FETs **515** and **520**. The gate of each FET **515** is coupled to receive the PBIAS signal, which biases the FET **515** to act as weak pull-up devices. Thus, the positive rails of the inverters are charged slowly and require little current. The FETs **520** act as cascode devices that isolate the positive rails of the inverters from the operating supply voltage VCC when the voltage at the gate

of the FET **520** is logic high. Each of the FETs **520** is controlled independently of the other FETs **520**. Generally, the gates of the FETs **520** are controlled by the output of the inverter that is one more than one-half the total number of inverters down the chain from the output of the corresponding inverter. For example, the FET **520** coupled to the inverter **460** has its gate voltage controlled by the output of inverter **490**, wherein the FET **520** coupled to the inverter **465** has its gate voltage controlled by the output of inverter **495**.

The negative rails of the inverters **460–510** are similarly coupled to system ground VSS via n-channel FETs **525** and **530**. The gates of FETs **525** are all coupled to the NBIAS signal such that the FETs **525** operate as weak pull-down devices. Each of the FETs **530** is controlled independently of the other FETs **530**. Generally, the gates of the FETs **530** are controlled by the output of the inverter that is one more than one-half the total number of inverters down the chain from the output of the corresponding inverter. For example, the FET **530** coupled to the inverter **460** has its gate voltage controlled by the output of inverter **490**, wherein the FET **530** coupled to the inverter **465** has its gate voltage controlled by the output of inverter **495**.

One advantage of biasing the pull-up and pull-down devices (FETs **515** and **525**) of the oscillators to be in the subthreshold region is that the frequency of the oscillators tends to increase with temperature. This should be contrasted with pull-up and pull-down devices that are biased to operate in the saturated region, wherein the frequency of the oscillator tends to decrease with temperature. The leakage current of the wordline switches **23** also tends to increase with temperature, and the increased frequency of the oscillators allows the wordline switches **23** to be maintained at approximately five volts.

The cascode devices **520** and **530** coupled to the rails of each inverter help to ensure that no conduction path is provided between VCC and VSS. Wherein it is possible that the p-channel and n-channel FETs (not shown) of the inverters may be switched on simultaneously for a short period of time when the inverter transitions from one state to another, the cascode devices **520** and **530** effectively eliminate any conduction path between VCC and VSS because either VCC or VSS is decoupled from the inverter. It is also possible for the cascode devices **520** and **530** to be switched on simultaneously when the output of the controlling inverter transitions from one state to another; however, the inverter for which the FETs **520** and **530** act as cascode devices is in the steady state such that no conduction path between VCC and VSS arises.

The period of a ring oscillator is equal to the twice the product of the total number of inverters and the propagation delay for an inverter. For one embodiment, the low frequency oscillator **450** is selected to have a period of three milliseconds.

Returning to FIG. **21**, the output of the low frequency oscillator **450** is provided to enable the high frequency oscillator **455**. The high frequency oscillator **455** may be a ring oscillator similar to that shown in FIG. **22**, wherein the period is defined to be much smaller than that of the low frequency oscillator **455**. The period of the high frequency oscillator **455** may be, for example, twelve microseconds. The high frequency oscillator **455** is enabled to begin operation when the output of the low frequency oscillator **450** goes high. The output of the high frequency oscillator **455** is fed back to the input of the high frequency oscillator **455** so that the high frequency oscillator **455** may be disabled when the output of the high frequency oscillator **455** goes low. In this manner, a single pulse having a duration of half the period of the small period oscillator is generated at the once every large period.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

What is claimed is:

1. A circuit for generating one of a plurality of output voltages, comprising:

a first conductor coupled to a first supply voltage;

a second conductor coupled to a second supply voltage;

a charge pump having an input and an output;

a multiplexor having a first input, a second input, and an output coupled to the input of the charge pump, the multiplexor for coupling a selected one of the first and the second inputs of the multiplexor to the output of the multiplexor;

a first regulation circuit coupled to the first input of the multiplexor and the output of the charge pump, the first regulation circuit for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first output voltage when the first input of the multiplexor is coupled to the output of the multiplexor; and

a second regulation circuit coupled to the second input of the multiplexor and the output of the charge pump, the second regulation circuit for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second output voltage when the second input of the multiplexor is coupled to the output of the multiplexor.

2. The circuit for generating one of a plurality of output voltages as claimed in claim **1**, wherein the first regulation circuit comprises:

a first voltage reference circuit coupled to the first supply voltage, the first voltage reference circuit for generating a first reference voltage in response to the first supply voltage; and

a voltage controlled oscillator having a positive terminal coupled to receive the first reference voltage and a negative terminal coupled to the output of the charge pump, the voltage controlled oscillator for outputting the first regulation voltage in response to the first voltage.

3. The circuit for generating one of a plurality of output voltages as claimed in claim **2**, wherein the charge pump comprises:

an oscillator coupled to the output of multiplexor, the oscillator for generating a clock signal in response to a one of the first and second regulation voltages;

a first clock driver circuit coupled to receive the clock signal for outputting a first phase of the clock signal;

a second clock driver circuit coupled to receive the clock signal for outputting a second phase of the clock signal;

a boost circuit coupled to receive the first phase of the clock signal, the second phase of the clock signal, and the first supply voltage, the boost circuit for outputting the first output voltage in response to the first phase of

the clock signal, the second phase of the clock signal and the first supply voltage.

4. The circuit for generating a plurality of output voltages as claimed in claim 1, wherein the multiplexor comprises a third input that can be selectively coupled to the output of the multiplexor, the circuit further comprising:

a third regulation circuit coupled to the third input of the multiplexor and the output of the charge pump, the third regulation circuit for generating a third regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a third output voltage when the third input of the multiplexor is coupled to the output of the multiplexor.

5. A circuit for generating one of a plurality of output voltages, comprising:

a first conductor coupled to a first supply voltage;

a first switch having a first terminal and a second terminal, wherein the first terminal of the first switch is coupled to the first conductor;

a second conductor coupled to a second supply voltage;

a second switch having a first terminal and a second terminal, wherein the first terminal of the second switch is coupled to the second conductor;

a charge pump having an input and an output;

a multiplexor having a first input, a second input, and an output coupled to the input of the charge pump, the multiplexor for coupling a selected one of the first and second inputs of the multiplexor to the output of the multiplexor;

a first regulation circuit coupled to the second terminal of the first switch, the first input of the multiplexor, and the output of the charge pump, the first regulation circuit for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first voltage when the first input of the multiplexor is coupled to the output of the multiplexor;

a second regulation circuit coupled to the second terminal of the second switch, the second input of the multiplexor, and the output of the charge pump, the second regulation circuit for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second voltage when the second input of the multiplexor is coupled to the output of the multiplexor; and

a control circuit coupled to the first switch, the second switch, and the multiplexor, the control circuit for closing the first switch, opening the second switch, and causing the first input of the multiplexor to be coupled to the output of the multiplexor when the first output voltage is selected for output, and the control circuit for closing the second switch, opening the first switch, and causing the second input of the multiplexor to be coupled to the output of the multiplexor when the second output voltage is selected for output.

6. The circuit for generating one of a plurality of output voltages as claimed in claim 5, wherein the first regulation circuit comprises:

a first voltage reference circuit coupled to the first supply voltage, the first voltage reference circuit for generating a first reference voltage in response to the first supply voltage; and

a voltage controlled oscillator having a positive terminal coupled to receive the first reference voltage and a negative terminal coupled to the output of the charge pump, the voltage controlled oscillator for outputting the first regulation voltage in response to the first voltage.

7. The circuit for generating one of a plurality of output voltages as claimed in claim 6, wherein the charge pump comprises:

an oscillator coupled to the output of multiplexor, the oscillator for generating a clock signal in response to a one of the first and second regulation voltages;

a first clock driver circuit coupled to receive the clock signal for outputting a first phase of the clock signal;

a second clock driver circuit coupled to receive the clock signal for outputting a second phase of the clock signal;

a boost circuit coupled to receive the first phase of the clock signal, the second phase of the clock signal, and the first supply voltage, the boost circuit for outputting the first output voltage in response to the first phase of the clock signal, the second phase of the clock signal and the first supply voltage.

8. The circuit for generating a plurality of output voltages as claimed in claim 5, wherein the multiplexor comprises a third input that can be selectively coupled to the output of the multiplexor, the circuit further comprising:

a third regulation circuit coupled to the third input of the multiplexor and the output of the charge pump, the third regulation circuit for generating a third regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a third output voltage when the third input of the multiplexor is coupled to the output of the multiplexor.

9. A nonvolatile memory device comprising:

a first conductor coupled to a first supply voltage;

a second conductor coupled to a second supply voltage;

a charge pump having an input and an output;

a memory cell array coupled to the output of the charge pump, the memory cell array comprising a plurality of nonvolatile memory cells arranged in a plurality of rows and columns;

a multiplexor having a first input, a second input, and an output coupled to the input of the charge pump, the multiplexor for coupling a selected one of the first and the second inputs of the multiplexor to the output of the multiplexor;

a first regulation circuit coupled to the first input of the multiplexor and the output of the charge pump, the first regulation circuit for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first output voltage when the first input of the multiplexor is coupled to the output of the multiplexor; and

a second regulation circuit coupled to the second input of the multiplexor and the output of the charge pump, the second regulation circuit for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second output voltage when the second input of the multiplexor is coupled to the output of the multiplexor.

10. The nonvolatile memory device of claim 9, wherein the first regulation circuit comprises:

a first voltage reference circuit coupled to the first supply voltage, the first voltage reference circuit for generating a first reference voltage in response to the first supply

voltage; and

a voltage controlled oscillator having a positive terminal coupled to receive the first reference voltage and a negative terminal coupled to the output of the charge pump, the voltage controlled oscillator for outputting the first regulation voltage in response to the first voltage.

11. The nonvolatile memory device as claimed in claim **10**, wherein the charge pump comprises:

an oscillator coupled to the output of multiplexor, the oscillator for generating a clock signal in response to a one of the first and second regulation voltages;

a first clock driver circuit coupled to receive the clock signal for outputting a first phase of the clock signal;

a second clock driver circuit coupled to receive the clock signal for outputting a second phase of the clock signal;

a boost circuit coupled to receive the first phase of the clock signal, the second phase of the clock signal, and the first supply voltage, the boost circuit for outputting the first output voltage in response to the first phase of the clock signal, the second phase of the clock signal and the first supply voltage.

12. The nonvolatile memory device as claimed in claim **9** wherein the first output voltage is selected to read the array of memory cells and the second output voltage is selected to program the array of memory cells.

13. The nonvolatile memory device as claimed in claim **9**, wherein the multiplexor comprises a third input that can be selectively coupled to the output of the multiplexor, the circuit further comprising:

a third regulation circuit coupled to the third input of the multiplexor and the output of the charge pump, the third regulation circuit for generating a third regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a third output voltage when the third input of the multiplexor is coupled to the output of the multiplexor.

14. The nonvolatile memory device as claimed in claim **13** wherein the first output voltage is selected to read the array of memory cells, the second output voltage is selected to program the array of memory cells, and the third output voltage is selected to erase the array of memory cells.

15. A nonvolatile memory device comprising:

a first conductor coupled to a first supply voltage;

a first switch having a first terminal and a second terminal, wherein the first terminal of the first switch is coupled to the first conductor;

a second conductor coupled to a second supply voltage;

a second switch having a first terminal and a second terminal, wherein the first terminal of the second switch is coupled to the second conductor;

a memory cell array coupled to the output of the charge pump, the memory cell array comprising a plurality of nonvolatile memory cells arranged in a plurality of rows and columns;

a charge pump having an input and an output;

a multiplexor having a first input, a second input, and an output coupled to the input of the charge pump, the multiplexor for coupling a selected one of the first and second inputs of the multiplexor to the output of the multiplexor;

a first regulation circuit coupled to the second terminal of the first switch, the first input of the multiplexor, and the output of the charge pump, the first regulation circuit for generating a first regulation voltage in response to the first supply voltage and the output of the charge pump such that the charge pump outputs a first voltage when the first input of the multiplexor is coupled to the output of the multiplexor;

a second regulation circuit coupled to the second terminal of the second switch, the second input of the multiplexor, and the output of the charge pump, the second regulation circuit for generating a second regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge pump outputs a second voltage when the second input of the multiplexor is coupled to the output of the multiplexor; and

a control circuit coupled to the first switch, the second switch, and the multiplexor, the control circuit for closing the first switch, opening the second switch, and causing the first input of the multiplexor to be coupled to the output of the multiplexor when the first output voltage is selected for output, and the control circuit for closing the second switch, opening the first switch, and causing the second input of the multiplexor to be coupled to the output of the multiplexor when the second output voltage is selected for output.

16. The nonvolatile memory device of claim **15**, wherein the first regulation circuit comprises:

a first voltage reference circuit coupled to the first supply voltage, the first voltage reference circuit for generating a first reference voltage in response to the first supply voltage; and

a voltage controlled oscillator having a positive terminal coupled to receive the first reference voltage and a negative terminal coupled to the output of the charge pump, the voltage controlled oscillator for outputting the first regulation voltage in response to the first voltage.

17. The nonvolatile memory device as claimed in claim **16**, wherein the charge pump comprises:

an oscillator coupled to the output of multiplexor, the oscillator for generating a clock signal in response to a one of the first and second regulation voltages;

a first clock driver circuit coupled to receive the clock signal for outputting a first phase of the clock signal;

a second clock driver circuit coupled to receive the clock signal for outputting a second phase of the clock signal;

a boost circuit coupled to receive the first phase of the clock signal, the second phase of the clock signal, and the first supply voltage, the boost circuit for outputting the first output voltage in response to the first phase of the clock signal, the second phase of the clock signal and the first supply voltage.

18. The nonvolatile memory device as claimed in claim **15** wherein the first output voltage is selected to read the array of memory cells and the second output voltage is selected to program the array of memory cells.

19. The nonvolatile memory device as claimed in claim **15**, wherein the multiplexor comprises a third input that can be selectively coupled to the output of the multiplexor, the circuit further comprising:

a third regulation circuit coupled to the third input of the multiplexor and the output of the charge pump, the third regulation circuit for generating a third regulation voltage in response to the second supply voltage and the output of the charge pump such that the charge

pump outputs a third output voltage when the third input of the multiplexor is coupled to the output of the multiplexor.

20. The nonvolatile memory device as claimed in claim 19 wherein the first output voltage is selected to read the array of memory cells, the second output voltage is selected to program the array of memory cells, and the third output voltage is selected to erase the array of memory cells.

21. The circuit for generating one of a plurality of output voltages as claimed in claim 1, wherein the second conductor is the first conductor and the second supply voltage is the first supply voltage.

22. The circuit for generating one of a plurality of output voltages as claimed in claim 5, wherein the second conductor is the first conductor and the second supply voltage is the first supply voltage.

23. The nonvolatile memory device of claim 9, wherein the second conductor is the first conductor and the second supply voltage is the first supply voltage.

24. The nonvolatile memory device of claim 15, wherein the second conductor is the first conductor and the second supply voltage is the first supply voltage.

* * * * *

APPENDIX C

Cases Cited in Appeal Brief

Copies of the following references are attached hereto:

In re Ratti, 270 F.2d 810, 123 USPQ 349 (C.C.P.A. 1987).

In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002)

Nothing in §261 itself creates a right of in the federal courts seeking an inter- ion of contracts. BSI's repeated misla- of this action as one for "declaration of lidity of an assignment" cannot make basis for federal jurisdiction over this t suit.

aming the truth of what it wishes were ut is not, BSI presents a number of irrelevant, question-begging, and con- considerations: treaties allow foreign ils to obtain and assign U.S. patent 35 U.S.C. §102 refers to a "person" t specifying nationality; the Constitu- es not specify nationality of "authors ventors"; all U. S. citizens are affected 'assignment" of an application; a state annot decide "a federal right created eral statute"; Rasmussen and BSI's corporation are foreign entities; pat- grants of federal rights.

otness

ontends in its main brief that, because ubstitution, diversity jurisdiction now nd this appeal has thereby been ren- moot" or "probably moot". BSI did vever, move to withdraw the appeal. sen agreed that the appeal is moot in diversity. BSI's reply brief says only appeal is not procedurally frivolous otness because Rasmussen has not to a remand.

Beghin-Say assigned whatever rights ave in the two U. S. applications to the district court entered the order from in this case and BSI moved for ion *after* this appeal was filed. Those annot establish diversity jurisdiction strict court under §1332(a)(2) when laint was filed. That determination made as of the filing date of a t, or of an amended complaint, and changed by action of a party there- lbert v. Kevex Corp., Nos. 83- 221 USPQ 202 (Fed. Cir. March 6, is in any event a matter for decision istrict court in the first instance.[4] ion of diversity jurisdiction in BSI's suite, supra, note 3, if that oc- uld not work a retroactive creation y jurisdiction in the Virginina court

ant of BSI's motion for substitution on not constitute such substitution before court. If BSI persists in its apparent onduct two identical suits in two busy rts, it may file a new complaint in the urt, whereupon one of the duplicative , presumably, be stayed or transferred.

that issued the order here appealed from. Nor does substitution of BSI on appeal affect the sole issue before us, i.e., whether the Virginia district court erred in holding that it had no jurisdiction under §1338(a) over the action as filed. Nor would we have jurisdiction over an appeal from a final decision of a district court in a case in which that court's jurisdiction was based solely on diversity of citizenship.

As above indicated, we do have jurisdiction to decide our own jurisdiction and that of the district court on which our own depends. The appealed order was based on lack of jurisdiction over this type of suit under §1338(a). BSI questions the correctness of that order. Our decision disposes of that question and the appeal is not therefore moot.

(4) Costs

Rasmussen requests costs, attorney fees, and damages under Rule 38, Fed. R. App. P., asserting that this appeal is frivolous on its merits and in its procedural foundation and that it was filed for the sole purpose of unnecessarily and needlessly prolonging the ongoing conflict between the parties.

This court has noted that the filing of and proceeding with a clearly frivolous appeal constitutes an unnecessary and unjustifiable burden on overcrowded courts, diminishes the opportunity for careful contemplative consideration of non-frivolous appeals, and delays access to the courts of persons having truly deserving causes. Asberry v. United States Postal Service, 692 F.2d 1378, 215 USPQ 921 (Fed. Cir. 1982); Connell v. Sears Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983). Asberry was called to counsel's attention when this appeal was filed.

There are, however, differences between excessive advocacy and inexperience on the one hand and clear frivolity on the other. True, it is difficult to conceive of any useful or non-frivolous purpose that could have reasonably motivated the continuation of this appeal, an appeal that does border the ragged edge of frivolity. First, BSI has a suit pending in Delaware, where it says diversity jurisdiction exists, and where a judgment on the merits may be obtained from which an appeal will lie to the United States Court of Appeals for the Third Circuit.[5] Second, the result of a reversal here, if there had been a remote chance of achieving it, would have been merely the pendency of BSI's two identical suits in two different federal district courts. Third, BSI continued to prosecute the appeal after the bankruptcy of its arguments had been pointed out in Rasmussen's brief.

Though a total absence of merit in BSI's arguments may, as Rasmussen suggests, be viewed as evidence of frivolousness, it may in this case also be viewed as the product of other factors, as indicated above. That consideration argues against Rasmussen's demand for all sanctions possible under Rule 38. Another sanction-limiting factor is an opportunity provided for guidance to the parties. BSI may now, for example, deem advisable the removal of §1338(a) as a claimed basis for jurisdiction in the district court for Delaware, and may also recognize that the sole basis for jurisdiction over this contract suit in any federal district court is diversity of citizenship.

We decline therefore to grant Rasmussen's request for a total sanction, including attorney fees and damages. We do order that BSI shall reimburse Rasmussen for his costs on this appeal.

Decision

Because no jurisdiction of the district court was here based on §1338(a), the appeal must be dismissed for lack of jurisdiction in this court.

Costs to Rasmussen.

Dismissed

Friedman, Circuit Judge, concurs in the result.

[5] If trial of this action in either district court proceeds to conclusion, the court will decide the case in accordance with the law of contracts, which may be that of the appropriate state; see In Re Snap-On Tools, 720 F.2d 654, 220 USPQ 8 (Fed. Cir. 1983), or, perhaps, that of France.

Court of Appeals, Federal Circuit

In re Gordon et al.

No. 83-1281

Decided May 10, 1984

PATENTS

1. Patentability — Anticipation — Modifying references (§51.217)

Question is not whether patentable distinction is created by viewing prior art apparatus

from one direction and claimed apparatus from another, but whether it would have been obvious from fair reading of prior art reference as whole to turn prior art apparatus upside down; mere fact that prior art could be modified by turning apparatus upside down does not make modification obvious unless prior art suggested desirability of modification.

Particular patents — Blood Filters

Gordon and Sutherland, Blood Filter Assembly, Rejection of claims 1-3 and 5-7 reversed.

Application for patent of Lucas S. Gordon and Karl M. Sutherland, Serial No. 124,312, filed Feb. 25, 1980. From decision rejecting claims 1-3 and 5-7, applicants appeal. Reversed.

James W. Geriak, Los Angeles, Calif. (Bradford J. Duft, Los Angeles, Calif., on the brief) for appellants.

John F. Pitrelli (Joseph F. Nakamura and John W. Dewhurst, on the brief) for Patent and Trademark Office.

Before Bennett and Miller, Circuit Judges and Skelton, Senior Circuit Judge.

Miller, Circuit Judge.

This appeal is from the decision of the United States Patent and Trademark Office ("PTO") Board of Appeals ("board") affirming the examiner's rejection of appellants' claims[1] 1-3 and 5-7 as unpatentable under 35 U.S.C. §103. We reverse.

The Invention

Appellants claim a "blood filter assembly" used during surgery and other medical procedures involving the handling of blood to remove clots, bone debris, tissue, or other foreign materials from blood before it is returned to a patient's body. Unlike blood filter assemblies widely used in the prior art, the device of the present invention permits both entry of the blood into, and ultimate discharge of the blood out of, the *bottom* end of the filter assembly, as shown below.[2]

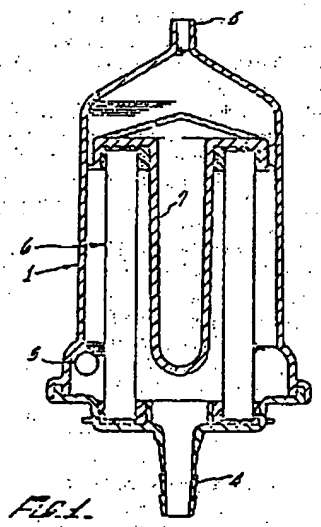


Fig. 1

The blood filter assembly comprises a shell 1 provided with blood inlet 3 and blood outlet 4. Between the blood inlet and the blood outlet is filter medium 6 positioned within the filter medium core 7.

The location of blood inlet 3 is such that the incoming blood is directed along a spirally upward path by the inner wall of the shell. Further, the location of the blood inlet at the bottom end of the filter assembly facilitates the removal of gas bubbles by allowing them to rise upwardly out of the blood. The gas bubbles so removed are released from the blood filter assembly by means of a gas vent 5 located in the region of the top end of the assembly.

Independent claim 1, from which the other appealed claims depend, is illustrative:

> Blood filter assembly comprising:
>
> a. a shell having a first top end and a second bottom end,
>
> b. a blood inlet located in the region of said bottom end and opening into said bottom end,
>
> c. a blood outlet located in the region of said bottom end,
>
> d. a gas vent located in the region of said top end, and
>
> e. a blood filter medium located between said blood inlet and said blood outlet,
>
> said blood inlet being located and configured in a manner capable of directing incoming blood in a generally spiral path within said shell.

Claims 2, 3, and 5-7 further define the shape of the shell, the shape of the filter medium, and the nature of the material used as the filter medium.

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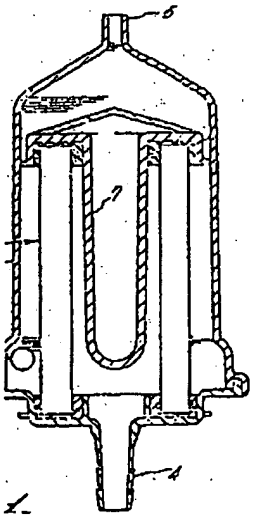
[1] In application Serial No. 124,312, filed February 25, 1980, for a "Blood Filter."

[2] Extraneous numbers have been removed from this and the subsequent drawing for clarification.



ter assembly comprises a shell 1
h blood inlet 3 and blood outlet
the blood inlet and the blood
medium 6 positioned within the
core 7.

on of blood inlet 3 is such that
blood is directed along a spirally
by the inner wall of the shell.
location of the blood inlet at the
of the filter assembly facilitates
of gas bubbles by allowing them
rdly out of the blood. The gas
removed are released from the
ssembly by means of a gas vent 5
ie region of the top end of the

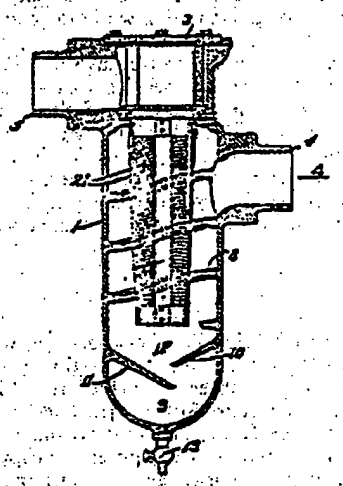
nt claim 1, from which the other
ims depend, is illustrative:

lter assembly comprising:
:ll having a first top end and a
tom end,
od inlet located in the region of
m end and opening into said
d,
od outlet located in the region of
n end,
vent located in the region of said
nd
od filter medium located between
inlet and said blood outlet,
od inlet being located and con-
a manner capable of directing
blood in a generally spiral path
d shell.

and 5-7 further define the shape
the shape of the filter medium,
ure of the material used as the
n.

Prior Art

The sole reference relied upon by the board is United States Patent No. 1,175,948, issued March 21, 1916, to French. French discloses a liquid strainer for removing dirt and water from gasoline and other light oils. As shown below, the inlet 4 and outlet 5 of the French device are both at the *top* end of the device.



A continuous helical tooth or thread 8 is formed integral with the inner wall of shell 1 and imparts to the incoming liquid a whirling motion, which gives the liquid a scouring action to help clean the surface of a metal screen filter 21 and guides unwanted dirt and water downwardly into a pocket 9 in the bottom of the shell. A pair of shelves 10 and 11, projecting inwardly and downwardly from the inner wall of the shell, further assists the entrance of dirt and water into the pocket 9 and prevents their being drawn back into the main chamber 12. The reference expressly states, "gravity assists in the separation of heavier oils or water." A pet-cock 13, projecting vertically downward from the bottom of the pocket is used to remove the collected dirt and water periodically. The top of the liquid strainer is completely closed by gland 3 except for the inlet and outlet openings.

Board Opinion

The board held that the appealed claims were drawn to an apparatus which "would have at least been rendered prima facie obvious to one of ordinary skill in the art by the apparatus disclosed in French." The board's reasoning was that it would have been obvious to turn the French device upside down to have both the inlet and outlet at the bottom, rather than at the top; and to employ French's "pet-cock" as the claimed "gas vent." In the board's opinion, no patentable distinction was created by viewing French's apparatus from one direction and the claimed apparatus from another.

ANALYSIS

[1] We are persuaded that the board erred in its conclusion of prima facie obviousness. The question is not whether a patentable distinction is created by viewing a prior art apparatus from one direction and a claimed apparatus from another, but, rather, whether it would have been obvious from a fair reading of the prior art reference as a whole to turn the prior art apparatus upside down. French teaches a liquid strainer which relies, at least in part, upon the assistance of gravity to separate undesired dirt and water from gasoline and other light oils. Therefore, it is not seen that French would have provided any motivation to one of ordinary skill in the art to employ the French apparatus in an upside down orientation. The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification. See Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983), and In re Sernaker, 702 F.2d 989, 995-96, 217 USPQ 1, 6-7 (Fed. Cir. 1983), both citing In re Imperato, 486 F.2d 585, 587, 179 USPQ 730, 732 (CCPA 1973).

Indeed, if the French apparatus were turned upside down, it would be rendered inoperable for its intended purpose. The gasoline to be filtered would be trapped in pocket 9, and the water French seeks to separate would flow freely out of the outlet 5. Further, unwanted dirt would build up in the space between the wall of shell 1 and screen 21, so that, in time, screen 21 would become clogged unless a drain valve, such as pet-cock 13, were re-introduced at the new "bottom" of the apparatus. See In re Schulpen, 390 F.2d 1009, 1013, 157 USPQ 52, 55 (CCPA 1968). In effect, French teaches away from the board's proposed modification.

Because the PTO has failed to establish a prima facie case of obviousness, the rejection of claims 1-3 and 5-7 as unpatentable under 35 U.S.C. §103 must be *reversed*.[1]

Reversed

[1] Because our holding that the PTO has failed to establish a prima facie case is dispositive, it is unnecessary to reach other arguments raised by appellants.

use and Senate reports on the bill ich became the Patent Act of 1952 2nd Cong., House Report No. 1923, y 12, 1952, p. 4; Senate Report No. 9, June 27, 1952, p. 3, to accompany R. 7794), it is quite unlikely that authors of the Constitution had pat- s, inventors or inventions in mind en in Art. 1, section 8 they referred "science." What we now know as ience" did not exist when the Consti- ion was written. Such "science" as sted was more likely to be called ural philosophy and the probability hat "science" in the Constitution re- red to knowledge in general, which s to be promoted by Congress, should choose to exercise its power, by curing for limited times to authors * the exclusive right to their * * * tings." See Karl B. Lutz, "Patents Science," 18 Geo. Wash. L.Rev. 50, J.P.O.S. 83, Feb. 1950. Thus there no implication that patents were to granted for scientific discoveries, or otheses, but only to inventors for r discoveries in useful arts. Hence statutory requirement that some- g of use in the useful arts must be luced and the correlative requirement it must be fully disclosed so that e in the art can use it.

ut in another way, the statutes do provide for the granting of patents ll *inventions*, which term could con- ably include the discovery of scien- facts or the invention of theories, only for patenting operative proc- s, machines, manufactures, composi- s of matter and improvements there- as accomplished facts, not mere osals.

ie record here shows that the useful waited a long time and for a vast int of work to be done subsequent ppellants' application disclosures be- a useful nuclear reactor or process roducing nuclear energy, for in- rial purposes, came into being. It is accomplishments of this sort that its are granted, and then provided that there is a disclosure of how hieve them.

46 CCPA 976

Court of Customs and Patent Appeals

In re RATTI

Appl. No. 6452 Decided Sept. 30, 1959

PATENTS

1. Evidence—Judicial notice (§ 36.20)

It is common knowledge that resilient deformable materials such as natural or synthetic rubber are incompressible, i.e., while they may be deformed, this can occur only if design and mounting of part permits resilient material to change its shape in response to applied forces.

2. Patentability — Anticipation — Combining references (§ 51.205)

Patentability — Anticipation — Modifying references (§ 51.217)

Combination of J patent with C patent is not proper ground for rejection of claims since combination would require substantial reconstruction and redesign of elements shown in C as well as change in basic principles under which C construction was designed to operate; once applicant taught how this could be done, redesign may, by hindsight, seem to be obvious to one having ordinary skills in art, but, when viewed as of time applicant's invention was made, and without benefit of applicant's disclosure, court finds nothing in art of record which suggests applicant's novel device.

3. Court of Customs and Patent Appeals —Issues determined—Ex parte patent cases (§ 28.203)

Rejection reversed by Board is not before court.

4. Patentability—In general (§ 51.01)

Novelty alone is not enough for patentability.

5. Patent grant—In general (§ 50.01)

Applicant is entitled to patent, under the statutes, unless one of the prohibitory provisions of statutes applies.

6. Patentability—In general (§ 51.01)

Patentability—Evidence of—In general (§ 51.451)

Patentability—Utility (§ 51.75)

Statutory requirements for patentability are novelty, usefulness, and unobviousness, as provided in 35 U.S.C. 101, 102, and 103; while proof that invention is better or possesses advantages may be persuasive of existence of any one or all of the requirements, and hence be indicative of patentability, Congress has not made such proof a prerequisite to patentability; moreover, Congress has never required that each and every patentable invention involve "progress" in the sense that it must possess some definite advantage over prior art; hence, it is improper to reject claim on ground that it does not possess some definite advantage over prior art; while R.S. 4893 may be said to have given Commissioner some discretion in refusing to grant patent on an otherwise patentable invention unless "the same is sufficiently useful and important," Congress removed this provision from new 35 U.S.C. 131; this is further indication that it is intent of Congress that patentability be determined solely by sections 101, 102, and 103.

7. Court of Customs and Patent Appeals —In general (§ 28.01)

Pleading and practice in Patent Office —In general (§ 54.1)

It is duty of Patent Office and Court of Customs and Patent Appeals to apply law as Congress wrote it.

Particular patents—Oil Seal

Ratti, Oil Seal, claims 1, 4, 7, and 10 of application allowed.

Appeal from Board of Appeals of the Patent Office.

Application for patent of Ferdinand J. Ratti, Serial No. 359,325, filed June 3, 1953; Patent Office Division 52. From decision rejecting claims 1, 4, 7, and 10, applicant appeals. Reversed; Kirkpatrick, Judge, dissenting with opinion in which Worley, Chief Judge, joins.

CROMWELL, GREIST & WARDEN (RAYMOND L. GREIST of counsel) both of Chicago, Ill., for appellant.

CLARENCE W. MOORE (S. WM. COCHRAN of counsel) for Commissioner of Patents.

Before WORLEY, Chief Judge, RICH, MARTIN, and SMITH, Associate Judges, and KIRKPATRICK, Judge *.

SMITH, Judge.

This is an appeal from the decision of the Board of Appeals of the United States Patent Office affirming the rejection by the Primary Examiner of claims 1, 4, 7 and 10 of appellant's application serial No. 359,325, filed June 3, 1953, for a patent on an "Oil Seal" for sealing the space between a bore in a housing and a relatively movable shaft centrally located in the bore.

* United States Senior District Judge for the Eastern District of Pennsylvania, designated to participate in place of Judge O'CONNELL, pursuant to the provisions of Title 28, United States Code, Section 294(d).

Claim 1 is representative of claims 4 and 7 and reads:

1. A seal for insertion in a cylindrical bore in a housing about a relatively movable centrally located shaft, comprising an annular bore-engaging mounting portion of resiliently deformable material for endwise insertion in and statically sealed engagement with the bore in the housing, an annular shaft-engaging portion connected with said bore-engaging portion for running engagement with the shaft, and a *metal ring* located adjacent one end of said bore-engaging portion, said ring being *provided with a plurality of axially extending outwardly biased spring fingers in outwardly clamped engagement with said bore-engaging portion* inwardly of the outer periphery of the latter, and said ring being *also provided* outwardly of said bore-engaging portion *with means for detachably connecting the ring to the housing* outwardly of the bore in the latter. (Emphasis ours.)

Claim 10 differs from the other claims on appeal and reads:

10. A seal for insertion in a cylindrical bore in a housing about a relatively movable centrally located shaft, comprising a sealing ring having an outer bore-engaging portion of resiliently deformable material, which portion is of somewhat larger diameter than the bore in the housing, for press-fit insertion in the bore, and a *metal retaining ring* associated with the sealing ring, said retaining ring being connected with the sealing ring and being provided outwardly of the latter *with resiliently yieldable hook formations which are adapted to be sprung into interlocking engagement with a complementary formation associated with the housing outwardly* of the bore, which engagement acts to prevent axial displacement of the sealing ring relative to the bore in the housing. (Emphasis ours.)

The references in the case are:

Roth, 1,546,942, July 21, 1925.
Norton, 1,951,034, Mar. 1, 1934.
Jepson, 2,544,824, Mar. 6, 1951.
Chinnery et al. (British), 578,526, July 2, 1946.

Appellant's shaft seal comprises an annular sealing member of resilient deformable material which is adapted to be inserted into a cylindrical bore surrounding a relatively movable shaft. The inner portion of the sealing member is provided with a flexible lip which is held in engagement with the shaft by a garter spring. In the outer portion of the sealing member, an annular slot is provided which is concentric with and spaced from the outer periphery of the sealing member. This slot extends axially from the end of the member and provides a pocket in which the axially extending outwardly biased spring fingers of a metallic attaching ring are located. This construction permits the spring fingers to exert a force on the resilient material in the direction of the annular wall of the bore to provide and maintain a snug engagement between the outer surface of the resilient member and the inner surface of the bore. The metallic attaching ring is also provided with radially extending resilient hooks located outwardly of the bore engaging portion of the resilient member. The housing is provided with a complementary formation outwardly of the bore which is engaged by the resilient hooks to provide a snap-on connection between the bore and the seal.

The Roth and Norton patents were relied upon by the examiner in rejecting claim 10, and since both references were considered by the board, we have included them in our consideration of this case. Roth shows a gasket structure for steam train line hose couplings. Norton shows an adjustable repair clamp for bell and spigot joints in which there is provided a sheet metal bridge piece "preferably of spring material." The bridge piece is sprung into interlocking engagement with a structural portion of the clamp and exerts its force on a resilient packing ring which, if desired, may be cemented to it.

The Chinnery et al. patent is the reference principally relied upon by the Patent Office. It shows a housing provided with a bore surrounding a centrally located shaft. A reinforced and "stiffened" sealing member formed of a material such as rubber, is press fitted into the space between the bore and the shaft. The sealing member has an inner lip held in contact with the shaft by a garter spring. The bore engaging portion of the sealing member is "stiffened" by an axially extending cylindrical sheet metal casing which acts as a reinforcing member for a definite purpose which is described by Chinnery et al. as follows:

> Owing to the limited radial space within which the oil seal is to be accommodated, the holding portion of the oil seal cannot be stiffened by being massive. Consequently the holding portion of the present oil seal is stiffened in the known manner by a reinforcement, which may either encase or line, or alternatively constitute, such holding portion and therefore makes the press-fitting contact with the machine part stationary relatively thereto, *or may be an internal reinforcement in the sense that it does not make press-*

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fitting contact with the machine part stationary relatively thereto. (Emphasis ours.)

In Fig. 8 Chinnery et al. shows a radially extending flange at the outer edge of a reinforcing member of the internal reinforcement type which flange extends beyond the sealing member "to such an extent as to serve as a means of attachment of the oil seal to the housing *i*, additional to the interference press fit of the holding portion *a* in the housing recess *g*." The aforesaid flange is shown attached to the housing by screws or bolts.

The Jepson patent relates to a gasket for sealing the space between the upper and lower vessels of a vacuum-type coffee maker. The gasket is an annular rubber member attached to the lower part of the upper vessel and is designed to fit into the upper part of the lower one. Located in a groove in the gasket is a sleeve member provided with axially and downwardly extending spring fingers which are so biased radially as to urge the lower peripheral portion of the gasket outwardly, thus effecting a tight engagement with the mouth of the lower vessel.

Claims 1, 4, and 7 stand rejected on Chinnery et al. in view of Jepson, on the ground that it would not require "invention" to replace the cylindrical sheet metal reinforcing member, which is secured to the Chinnery et al. sealing member, by an annular set of outwardly biased spring fingers shown by Jepson.

The problems which were solved by appellant's invention existed in this art at the time of his invention despite the Chinnery et al. disclosures. It was appellant rather than Chinnery et al. who provided the art with a shaft seal in which the resilient element of the seal could be readily inserted into a bore in the housing so that it could be removed from the bore and replaced by a new sealing element without mutilation of the sealing surface of the bore. This is particularly important, the specification points out, where the bore is formed in light metal alloys such as are used in aircraft engines and which are relatively soft and easily damaged. In appellant's oil seal, the resilient seal is so constructed that when mounted in the bore, it will establish and maintain a fluid tight relationship between the outer peripheral surface of the resilient seal member and the inside of the bore. Where either natural or synthetic rubber is used as the resilient sealing member in such seals, the rubber in time will take a set or lose its resiliency at least to the extent that the seals soon become ineffective to prevent leakage of oil. When subjected to mechanical pressures and heat, such a rubber sealing element loses its sealing effectiveness at an accelerated rate. The problems in the oil sealing art arising from such use of resilient sealing elements appear to have persisted because of the failure of the art to recognize these characteristics of the rubber sealing element and to so design the resilient element and the mounting therefor as to assure holding the outer circumference of the resilient sealing element in static oil-sealing contact with the inner circumference of the bore in which it is inserted.

Appellant's seal differs from the art of record in at least three respects:

(1) The provision of the annular slot which extends axially inward from one end of the resilient sealing element. This feature is claimed as part of the combination set forth in claim 4.

(2) The outwardly biased resilient spring means or fingers inserted in the resilient sealing element. These means are claimed as part of the combination of claims 1, 4 and 7.

(3) The "snap-on" connector which holds the resilient sealing element and engages with a complementary formation associated with the housing outwardly of the bore. This feature is in the combination of claim 10.

The patents cited by the examiner, either alone or in combination, do not disclose a resilient shaft sealing element having these features.

[1] It is common knowledge that resilient deformable materials such as either natural or synthetic rubber are incompressible, that is, while they may be deformed, this can occur only if the design and mounting of the part permits the resilient material to change its shape in response to the applied forces.

The seal construction disclosed in Chinnery et al. is such that the "interference press fit" which that patent calls for is alone relied on to keep the seal tight. There is nothing in the Chinnery et al. patent to show how the resilient sealing element is *maintained* in resilient contact with the bore otherwise than by the resiliency of the rubber. If and when that resiliency is lost, the sealing effect will be impaired.

Considering the incompressible nature of the rubber in the sealing element disclosed in Chinnery et al., its stiffening and reinforcement by the cylindrical sheet metal member, and its "interference press fit" in the bore, it seems clear to us that the Chinnery et al. seal cannot function in the manner of appellant's seal. Now, as to the contention that Jepson would suggest inserting a set of spring fingers, the resilient element of Chinnery et al. is forced so tightly into the bore

and is so "stiffened" that the use of the resilient spring fingers of Jepson could not possibly increase the resilient deformation of the Chinnery et al. seal in the direction of the bore or increase the sealing engagement of the seal with the bore. The teaching of the Chinnery et al. patent points away from the addition of any spring element. On the other hand, we find nothing in the disclosure of Jepson's coffee maker gasket to suggest that any part of it has applicability to shaft seals. The two arts are at least somewhat remote from each other even if they both involve sealing.

[2] We, therefore, find that Chinnery et al. did not teach the shaft sealing art how to solve the problems which existed in that art at the time of appellant's invention. We hold, further, that the combination of Jepson with Chinnery et al. is not a proper ground for rejection of the claims here on appeal. This suggested combination of references would require a substantial reconstruction and redesign of the elements shown in Chinnery et al. as well as a change in the basic principles under which the Chinnery et al. construction was designed to operate.

Once appellant had taught how this could be done, the redesign may, by hindsight, seem to be obvious to one having ordinary skills in the shaft sealing art. However, when viewed as of the time appellant's invention was made, and without the benefit of appellant's disclosure, we find nothing in the art of record which suggests appellant's novel oil seal as defined in claims 1, 4 and 7.

We shall now consider the rejection of claim 10, remarking first that it differs from claims 1, 4 and 7 in that it is directed to a combination of a housing bore, a resilient sealing ring and a metal retaining ring connected to the sealing ring, wherein the metal ring has *resilient hooks* which secure the seal in the bore. This claim is not limited to the outwardly biased spring fingers.

The examiner rejected claim 10 on two grounds: (1) that substitution for the screw securing means of Chinnery et al. of a series of spring hooks such as disclosed by Norton would not involve patentable invention, and (2) unpatentability over Roth.

[3] We shall first dispose of the second rejection. The board held that claim 10 is drawn to a combination of a sealing ring and a housing bore in which the sealing ring is detachably placed and that Roth discloses nothing of this nature. The board therefore reversed the rejection on Roth and consequently it is not before us.

As to the first rejection, the board recognized that it was on the ground of unpatentability "over Chinnery et al. in view of Norton" and pointed out that the examiner could see nothing patentable in substituting spring hook attaching means shown in Norton for the screws of Chinnery et al. It then said:

> Appellant argues that the references fail to suggest or teach how the proposed [claimed] combination could be made and after a careful consideration of the references, *we have concluded that he is correct in this respect. We therefore concede that the claim * * * defines novelty over the disclosure of Fig. 8 of Chinnery et al.* Novelty alone however, is no proper basis for the allowance of a claim. (Emphasis ours.)

[4] Although, in reaching this conclusion, the board made no reference to Norton, the context compels the conclusion that novelty was found notwithstanding the disclosure of Norton, taken together with Chinnery et al. We fully agree, of course, with the board's statement that novelty alone is not enough for patentability.

With the next statement of the board, in explanation of its affirmance of the rejection of claim 10, we do not agree. It reads:

> In order to *properly* define invention [meaning, of course, *patentable* invention], a claim should clearly define a structure *which possesses some definite advantage over the prior art.* As far as we can determine there is *no better* combination of housing and seal produced by using a series of snap fastener connections to connect the seal to the housing, as in appellant's structure, over using a series of bolts, as in the structure shown by Chinnery et al. Both act to merely detachably connect one element to another element and as far as we can find are merely equivalent connecting means especially in the absence of any unexpected result *or advantage* being obtained, by using one means in preference to the other, on which the record before us is entirely silent. (Emphasis ours.)

If we may extract from the foregoing what we understand to be the essence of the board's position in the matter, it is that claim 10 is not patentable, though it defines a combination which is novel over the disclosures of the references, because the claimed combination has not been shown to be any better than, or to possess any advantage over, what was known to the art.

[5] As was pointed out in In re Stempel, Jr., 44 CCPA 820, 241 F.2d 755, 113 USPQ 77, an applicant is entitled to a patent, under the statutes, unless one of the prohibitory provisions of the statutes applies. The statutory requirements

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[6] for patentability, broadly stated, are novelty, usefulness and unobviousness, as provided in 35 U.S.C. sections 101, 102, and 103. While it is true that proof that an invention *is* better or *does* possess advantages may be persuasive of the existence of any one or all of the foregoing three requirements, and hence be indicative of patentability, Congress has not seen fit to make such proof a prerequisite to patentability.[1]

Appellant's invention, as defined in claim 10, has been held by the board to possess novelty over the disclosure of Chinnery et al. Just what the board thought about the pertinency of Norton is obscure but it seems to have regarded this reference as of little moment. Appellent in his brief here said that Norton was held by the board to have no bearing on the invention and the Patent Office brief said that the appellant was correct in so stating and that the court need not consider it. We are, therefore, virtually without any reference against claim 10 except Chinnery et al. and the rejection thereon is predicated solely on a theory of patentability we find to be outside of the patent statutes, namely, that the combination of claim 10 is, by reason of the use of spring retaining hooks instead of a series of bolts, *no better* than the combination of Chinnery et al. However [7] intriguing such a ground of rejection may be, it is the duty of the tribunals of the Patent Office and of this court to apply the law as Congress has written it. While the provisions of the former R.S. 4893 may be said to have given the Commissioner some discretion in refusing to grant a patent on an otherwise patentable invention unless "the same is sufficiently useful and important," when the Patent Codification Act of 1952 was enacted, Congress removed this provision from old section 36 of title 35, now section 131. We take this as a further indication that it is the intent of Congress that patentability be determined solely by the provisions of sections 101, 102 and 103. We therefore reverse the board on this ground of rejection of claim 10.

If the issue before us were whether or not the spring hooks *are* better than the Chinnery et al. bolts—and we consider this in the event we have misapprehended the position of the board—we would hold that they are, on the basis of what is disclosed in the application. This retaining means seems to possess many advantages over screws. Similarly, if the board was intending to say that the hooks and the bolts are merely equivalent connecting means and that claim 10 is unpatentable because its combination differs from the prior art only in the substitution of an equivalent for one element in an old combination, then we would also have to disagree since we think it is clear that the use of the spring hooks produces a result quite different from the bolts of Chinnery et al. On the record before us no reference relied on shows any spring hooks nor does it contain any support for the contention that bolts and spring hooks are equivalents.

For the foregoing reasons we reverse the rejection of claim 10.

The rejections of claims 1, 4, 7 and 10 are *reversed.*

MARTIN, Judge, concurs in result.

KIRKPATRICK, Judge, dissenting, in which WORLEY, Chief Judge, joins.

I think that the board's rejection of claims 1, 4 and 7 should be affirmed. The central idea and the most important feature of these three claims, as well as of allowed claim 5, is the exertion of outwardly directed pressure upon the bore engaging portion of the sealing member, the result accomplished being to counteract the tendency of rubber to "set" or lose its resiliency and so become ineffective to prevent leakage. Jepson comes very close to completely anticipating this feature of the patent. All that would be necessary to make the anticipation complete would be to provide the Jepson seal with a shaft engaging portion and, incidentally, claim 7 does not specify any shaft engaging portion.

Of course, it was necessary that the seal be attached to the bore in a manner to prevent its displacement. Chinnery provides a flange and screws for this purpose and none of the three claims referred to calls for anything more specific than "means." Thus it seems clear that

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[1] A critical essay on the existing law has recently appeared under the title "A Proposal for: A Standard of Patentability; Consonant Statutory Changes; A Manual on Determination of Patentability," by Malcolm F. Bailey, 41 J.P.O.S. 192-225, 231-257. It advocates, as we understand it, that the present law should be changed to set up as the test for patentability, in place of the requirement of section 103 that an invention be unobvious, a requirement that the invention involve *progress,* which the author finds in the constitutional provisions. Congress has not seen fit to include in the statutes, at any time during the past 169 years so far as we are aware, a requirement that each and every patentable *invention* shall involve "progress" in this sense, i.e., that each new invention must also be shown to possess some definite advantage over the prior art. The author relates the term "progress" to individual inventions and then gives it the connotation that each such invention should be a technical advance, improvement or betterment. The very making of the suggestion to change the law is an indication that the existing law is otherwise.

claims 1, 4 and 7 show no patentable novelty as against the prior art of Chinnery plus Jepson.

The only question is whether Jepson is in a nonanalogous art sufficiently remote from that of the application to put it beyond the probability that it would be considered by persons skilled in the art endeavoring to solve the problem to the solution of which the application is directed. I do not think that it is. Jepson was trying to meet exactly the same problem as the application under consideration, namely, to provide a compressible seal which could be readily detached or inserted in a cylindrical bore but which would maintain a firm and leakproof seat on the bore when in place. I agree with the Solicitor's argument that one seeking to improve a machinery seal would reasonably be expected to investigate not only machinery seals but seals in other arts where similar problems would be encountered. See In re O'Connor, 34 CCPA 1055, 161 F.2d 221, 73 USPQ 433.

Claim 10 stands on a somewhat different basis. This claim entirely omits what I think, and have stated above, to be the heart of the application. In substance, claim 10 really amounts to no more than a claim for a hook formation to interlock with the housing of a bore in order to hold a press fit seal in place.[1] Chinnery discloses means to serve the same purpose consisting of screws.

The board conceded that the combination disclosed in claim 10, consisting of spring hooks to fasten a press fit seal to the bore, disclosed novelty over Chinnery but not patentable novelty.

I do not read the opinion of the board as predicating its conclusion of want of invention on the theory that in order to be patentable a combination must have some distinct advantage over the prior art. The board stated that there was nothing in the record to show that the substitution of hooks for screws produced any unexpected result or advantage and, therefore, concluded that the introduction of hooks did not create patentable novelty, but was a mere substitution of equivalents. The statement that the spring hooks of Ratti were no better than the screws of Chinnery was directed toward this point and seemingly was added to fortify the board's finding of equivalency rather than to propound a theory of patentability. I agree with the board that this claim, though it may show novelty over Chinnery, does not show patentable novelty, and I would affirm its rejection.

[1] Chinnery discloses a press fit seal, but no one has suggested that there is anything new about such a device and the specification of the application before us concedes that it is old in the art.

Court of Claims of the United States

MYERS v. UNITED STATES

No. 119-56 Decided Nov. 4, 1959

PATENTS

1. Court of Claims—Jurisdiction (§ 27.5)

Former government employee may not maintain action under 28 U.S.C. 1498 where his employment as aeronautical engineer included research and development and, even assuming that development of his invention during employment was entirely on his own time with his own materials and facilities, invention related at least generally to official functions of his employment; it is unnecessary to decide actual date of completion of invention inasmuch as employee worked on idea during employment and constructively reduced invention to practice by filing patent application while employed; assertion that employee's superiors were not interested in idea does not warrant finding that idea did not relate to his official functions.

2. Court of Claims—Jurisdiction (§ 27.5)

Proviso in 28 U.S.C. 1498 bars right of action to employee-patentee with respect to any invention related to his official functions; it is not required that employee be specifically hired to make inventions or to make specific invention, or even that he be hired as inventor; if invention is made by employee, is related to his work, and his official functions include research and development, no right of action is conferred by proviso.

Particular patents—Aircraft

2,445,235, Myers, Aircraft with Blast or Like Tube and Closure Therefor, Court of Claims suit dismissed.

Petition by Joseph C. Myers against United States to recover compensation for use of invention. Petition dismissed.

SCOTT P. CRAMPTON (ROBERT F. CONRAD and WATSON, COLE, GRINDLE & WATSON on the brief) all of Washington, D.C., for plaintiff.

G. M. PADDACK and GEORGE COCHRAN DOUB for defendant.

PER CURIAM.

This case was referred pursuant to Rule 45(a) to Donald E. Lane, a trial

signs was not legally erroneous, and because we find that the Board's finding that Valu's guide rails are *de jure* functional is supported by substantial evidence, the Board's refusal to register Valu's guide rail designs is *affirmed*, and Rexnord's cross-appeal is dismissed as moot.

AFFIRMED

COSTS

No costs.

In re Lee

U.S. Court of Appeals
Federal Circuit
No. 00-1158
Decided January 18, 2002

PATENTS

[1] Practice and procedure in Patent and Trademark Office — Board of Patent Appeals and Interferences — In general (§ 110.1101)

Patentability/Validity — Obviousness — Combining references (§ 115.0905)

Patentability/Validity — Obviousness — Evidence of (§ 115.0906)

Rejection of patent application for obviousness under 35 U.S.C. § 103 must be based on evidence comprehended by language of that section, and search for and analysis of prior art includes evidence relevant to finding of whether there is teaching, motivation, or suggestion to select and combine references relied on as evidence of obviousness; factual inquiry whether to combine references must be thorough and searching, based on objective evidence of record, and Board of Patent Appeals and Interferences must explain reasons why one of ordinary skill in art would have been motivated to select references and to combine them to render claimed invention obvious.

[2] Patentability/Validity — Obviousness — Combining references (§ 115.0905)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

Board of Patent Appeals and Interferences improperly relied upon "common knowledge and common sense" of person of ordinary skill in art to find invention of patent application obvious over combination of two prior art references, since factual question of motivation to select and combine references is material to patentability, and could not be resolved on subjective belief and unknown authority, since deferential review of agency decisions under Administrative Procedure Act reinforces obligation of board to develop evidentiary basis for its findings, since board's rejection of need for any specific hint or suggestion in particular reference to support combination constituted omission of relevant factor required by precedent, and thus was both legal error and arbitrary agency action, since board's findings must extend to all material facts and be documented on record, and since "common knowledge and common sense" are not specialized knowledge and expertise of agency contemplated by APA, and may not be substituted for evidence, although they may be applied to analysis of evidence.

PATENTS

[3] Practice and procedure in Patent and Trademark Office — Board of Patent Appeals and Interferences — In general (§ 110.1101)

Patentability/Validity — Obviousness — Evidence of (§ 115.0906)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

Patent examiners and Board of Patent Appeals and Interferences, in relying on what they assert to be general knowledge to negate patentability on ground of obviousness, must articulate that knowledge and place it on record, since examiners and board are pre-

sumed to act from viewpoint of person of ordinary skill in art in finding relevant facts, assessing significance of prior art, and making ultimate determination of obviousness issue; failure to do so is not consistent with either effective administrative procedure or effective judicial review, and board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth rationale on which it relies.

[4] Procedure — Court of Appeals for the Federal Circuit (§ 410.03)

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

U.S. Court of Appeals for the Federal Circuit will not consider proposed alternative grounds for affirming decision of Board of Patent Appeals and Interferences rejecting patent application for obviousness, since alternative grounds were made at oral argument and constitute post hoc rationalization for agency action, consideration of which would deprive aggrieved party of fair opportunity to support its position.

Appeal from the U.S. Patent and Trademark Office, Board of Patent Appeals and Interferences.

Patent application of Sang-Su Lee, serial no. 07/631,210, directed to method of automatically displaying functions of video display device and demonstrating how to select and adjust functions to facilitate user response. Applicant appeals from decision upholding rejection of all claims for obviousness, and from reaffirmation of that decision on reconsideration. Reversed and remanded.

Richard H. Stern and Robert E. Bushnell, Washington, D.C., for Sang Su Lee.

Sidney O. Johnson Jr., associate solicitor, John M. Whealan, solicitor, and Raymond T. Chen, Maximilian R. Peterson, and Mark Nagumo, associate solicitors, Arlington, Va., for Director of U.S. Patent and Trademark Office.

Before Newman, Clevenger, and Dyk, circuit judges.

Newman, J.

Sang-Su Lee appeals the decision of the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office, rejecting all of the claims of Lee's patent application Serial No. 07/631,210 entitled "Self-Diagnosis and Sequential-Display Method of Every Function." [1] We vacate the Board's decision for failure to meet the adjudicative standards for review under the Administrative Procedure Act, and remand for further proceedings.

The Prosecution Record

Mr. Lee's patent application is directed to a method of automatically displaying the functions of a video display device and demonstrating how to select and adjust the functions in order to facilitate response by the user. The display and demonstration are achieved using computer-managed electronics, including pulse-width modulation and auto-fine-tuning pulses, in accordance with procedures described in the specification. Claim 10 is representative:

> 10. A method for automatically displaying functions of a video display device, comprising:
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> determining if a demonstration mode is selected;
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> if said demonstration mode is selected, automatically entering a picture adjustment mode having a picture menu screen displaying a list of a plurality of picture functions; and
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> automatically demonstrating selection and adjustment of individual ones of said plurality of picture functions.

The examiner rejected the claims on the ground of obviousness, citing the combination of two references: United States Patent No. 4,626,892 to Nortrup, and the Thunderchopper Helicopter Operations Handbook for a video game. The Nortrup reference describes a television set having a menu display by which the user can adjust various picture and audio functions; however, the Nortrup display does not include a demonstration of how to adjust the functions. The Thunderchopper Handbook describes the Thunderchopper game's video display as having a "demonstration mode" showing how to play the game; however, the Thunderchopper Handbook makes no mention of the adjustment of picture or audio functions. The examiner held that it

[1] *Ex parte Lee*, No. 1994-1989 (Bd. Pat. App. & Int. Aug. 30, 1994; on reconsid'n Sept. 29, 1999).

would have been obvious to a person of ordinary skill to combine the teachings of these references to produce the Lee system.

Lee appealed to the Board, arguing that the Thunderchopper Handbook simply explained how to play the Thunderchopper game, and that the prior art provided no teaching or motivation or suggestion to combine this reference with Nortrup, or that such combination would produce the Lee invention. The Board held that it was not necessary to present a source of a teaching, suggestion, or motivation to combine these references or their teachings. The Board stated:

> The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference.

Board op. at 7. The Board did not explain the "common knowledge and common sense" on which it relied for its conclusion that "the combined teachings of Nortrup and Thunderchopper would have suggested the claimed invention to those of ordinary skill in the art."

Lee filed a request for reconsideration, to which the Board responded after five years. The Board reaffirmed its decision, stating that the Thunderchopper Handbook was "analogous art" because it was "from the same field of endeavor" as the Lee invention, and that the field of video games was "reasonably pertinent" to the problem of adjusting display functions because the Thunderchopper Handbook showed video demonstrations of the "features" of the game. On the matter of motivation to combine the Nortrup and Thunderchopper references, the Board stated that "we maintain the position that we stated in our prior decision" and that the Examiner's Answer provided "a well reasoned discussion of why there is sufficient motivation to combine the references." The Board did not state the examiner's reasoning, and review of the Examiner's Answer reveals that the examiner merely stated that both the Nortrup function menu and the Thunderchopper demonstration mode are program features and that the Thunderchopper mode "is user-friendly" and it functions as a tutorial, and that it would have been obvious to combine them.

Lee had pressed the examiner during prosecution for some teaching, suggestion, or motivation in the prior art to select and combine the references that were relied on to show obviousness. The Examiner's Answer before the Board, plus a Supplemental Answer, stated that the combination of Thunderchopper with Nortrup "would have been obvious to one of ordinary skill in the art since the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software," and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial." The Board adopted the examiner's answer, stating "the examiner has provided a well reasoned discussion of these references and how the combination of these references meets the claim limitations." However, perhaps recognizing that the examiner had provided insufficient justification to support combining the Nortrup and Thunderchopper references, the Board held, as stated *supra*, that a "specific hint or suggestion" of motivation to combine was not required.

This appeal followed.

Judicial Review

Tribunals of the PTO are governed by the Administrative Procedure Act, and their rulings receive the same judicial deference as do tribunals of other administrative agencies. *Dickinson v. Zurko*, 527 U.S. 150, 50 USPQ2d 1930 (1999). Thus on appeal we review a PTO Board's findings and conclusions in accordance with the following criteria:

> 5 U.S.C. § 706(2) The reviewing court shall—
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> (2) hold unlawful and set aside agency actions, findings, and conclusions found to be—
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> (A) arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law;
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> (E) unsupported by substantial evidence in a case subject to sections 556 and 557 of this title or otherwise reviewed on the record of an agency hearing provided by statute;

For judicial review to be meaningfully achieved within these strictures, the agency tribunal must present a full and reasoned explanation of its decision. The agency tribunal

must set forth its findings and the grounds thereof, as supported by the agency record, and explain its application of the law to the found facts. The Court has often explained:

> The Administrative Procedure Act, which governs the proceedings of administrative agencies and related judicial review, establishes a scheme of "reasoned decisionmaking." Not only must an agency's decreed result be within the scope of its lawful authority, but the process by which it reaches that result must be logical and rational.

Allentown Mack Sales and Service, Inc. v. National Labor Relations Bd., 522 U.S. 359, 374 (1998) (citation omitted). This standard requires that the agency not only have reached a sound decision, but have articulated the reasons for that decision. The reviewing court is thus enabled to perform meaningful review within the strictures of the APA, for the court will have a basis on which to determine "whether the decision was based on the relevant factors and whether there has been a clear error of judgment." *Citizens to Preserve Overton Park v. Volpe*, 401 U.S. 402, 416 (1971). Judicial review of a Board decision denying an application for patent is thus founded on the obligation of the agency to make the necessary findings and to provide an administrative record showing the evidence on which the findings are based, accompanied by the agency's reasoning in reaching its conclusions. *See In re Zurko*, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) (review is on the administrative record); *In re Gartside*, 203 F.3d 1305, 1314, 53 USPQ2d 1769, 1774 (Fed. Cir. 2000) (Board decision "must be justified within the four corners of the record").

[1] As applied to the determination of patentability *vel non* when the issue is obviousness, "it is fundamental that rejections under 35 U.S.C. § 103 must be based on evidence comprehended by the language of that section." *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ 769, 775 (Fed. Cir. 1983). The essential factual evidence on the issue of obviousness is set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966) and extensive ensuing precedent. The patent examination process centers on prior art and the analysis thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. *See, e.g., McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the *Graham* factors).

"The factual inquiry whether to combine references must be thorough and searching." *Id.* It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. *See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding' ") (quoting *C.R. Bard, Inc., v. M3 Systems, Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (" 'teachings of references can be combined *only* if there is some suggestion or incentive to do so.' ") (emphasis in original) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).

The need for specificity pervades this authority. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combina-

tion. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); *In re Fritch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

[2] With respect to Lee's application, neither the examiner nor the Board adequately supported the selection and combination of the Nortrup and Thunderchopper references to render obvious that which Lee described. The examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Thus the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion.

Deferential judicial review under the Administrative Procedure Act does not relieve the agency of its obligation to develop an evidentiary basis for its findings. To the contrary, the Administrative Procedure Act reinforces this obligation. *See, e.g., Motor Vehicle Manufacturers Ass'n v. State Farm Mutual Automobile Ins. Co.*, 463 U.S. 29, 43 (1983) ("the agency must examine the relevant data and articulate a satisfactory explanation for its action including a 'rational connection between the facts found and the choice made.' ") (quoting *Burlington Truck Lines v. United States*, 371 U.S. 156, 168 (1962)); *Securities & Exchange Comm'n v. Chenery Corp.*, 318 U.S. 80, 94 (1943) ("The orderly function of the process of review requires that the grounds upon which the administrative agency acted are clearly disclosed and adequately sustained.").

In its decision on Lee's patent application, the Board rejected the need for "any specific hint or suggestion in a particular reference" to support the combination of the Nortrup and Thunderchopper references. Omission of a relevant factor required by precedent is both legal error and arbitrary agency action. *See Motor Vehicle Manufacturers*, 463 U.S. at 43 ("an agency rule would be arbitrary and capricious if the agency . . . entirely failed to consider an important aspect of the problem"); *Mullins v. Department of Energy*, 50 F.3d 990, 992 (Fed. Cir. 1995) ("It is well established that agencies have a duty to provide reviewing courts with a sufficient explanation for their decisions so that those decisions may be judged against the relevant statutory standards, and that failure to provide such an explanation is grounds for striking down the action."). As discussed in *National Labor Relations Bd. v. Ashkenazy Property Mgt. Corp.*, 817 F.2d 74, 75 (9th Cir. 1987), an agency is "not free to refuse to follow circuit precedent."

The foundation of the principle of judicial deference to the rulings of agency tribunals is that the tribunal has specialized knowledge and expertise, such that when reasoned findings are made, a reviewing court may confidently defer to the agency's application of its knowledge in its area of expertise. Reasoned findings are critical to the performance of agency functions and judicial reliance on agency competence. *See Baltimore and Ohio R. R. Co. v. Aberdeen & Rockfish R. R. Co.*, 393 U.S. 87, 91-92 (1968) (absent reasoned findings based on substantial evidence effective review would become lost "in the haze of so-called expertise"). The "common knowledge and common sense" on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation. This court explained in *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697, that "deficiencies of the cited references cannot be remedied by

the Board's general conclusions about what is 'basic knowledge' or 'common sense.' " The Board's findings must extend to all material facts and must be documented on the record, lest the "haze of so-called expertise" acquire insulation from accountability. "Common knowledge and common sense," even if assumed to derive from the agency's expertise, do not substitute for authority when the law requires authority. *See Allentown Mack*, 522 U.S. at 376 ("Because reasoned decisionmaking demands it, and because the systemic consequences of any other approach are unacceptable, the Board must be required to apply in fact the clearly understood legal standards that it enunciates in principle . . . .")

The case on which the Board relies for its departure from precedent, *In re Bozek*, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969), indeed mentions "common knowledge and common sense," the CCPA stating that the phrase was used by the Solicitor to support the Board's conclusion of obviousness based on evidence in the prior art. *Bozek* did not hold that common knowledge and common sense are a substitute for evidence, but only that they may be applied to analysis of the evidence. *Bozek* did not hold that objective analysis, proper authority, and reasoned findings can be omitted from Board decisions. Nor does *Bozek*, after thirty-two years of isolation, outweigh the dozens of rulings of the Federal Circuit and the Court of Customs and Patent Appeals that determination of patentability must be based on evidence. This court has remarked, in *Smiths Industries Medical Systems, Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1356, 51 USPQ2d 1415, 1421 (Fed. Cir. 1999), that *Bozek*'s reference to common knowledge "does not in and of itself make it so" absent evidence of such knowledge.

[3] The determination of patentability on the ground of unobviousness is ultimately one of judgment. In furtherance of the judgmental process, the patent examination procedure serves both to find, and to place on the official record, that which has been considered with respect to patentability. The patent examiner and the Board are deemed to have experience in the field of the invention; however, this experience, insofar as applied to the determination of patentability, must be applied from the viewpoint of "the person having ordinary skill in the art to which said subject matter pertains," the words of section 103. In finding the relevant facts, in assessing the significance of the prior art, and in making the ultimate determination of the issue of obviousness, the examiner and the Board are presumed to act from this viewpoint. Thus when they rely on what they assert to be general knowledge to negate patentability, that knowledge must be articulated and placed on the record. The failure to do so is not consistent with either effective administrative procedure or effective judicial review. The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies.

Alternative Grounds

[4] At oral argument the PTO Solicitor proposed alternative grounds on which this court might affirm the Board's decision. However, as stated in *Burlington Truck Lines, Inc. v. United States*, 371 U.S. 156, 168 (1962), "courts may not accept appellate counsel's *post hoc* rationalization for agency action." Consideration by the appellate tribunal of new agency justifications deprives the aggrieved party of a fair opportunity to support its position; thus review of an administrative decision must be made on the grounds relied on by the agency. "If those grounds are inadequate or improper, the court is powerless to affirm the administrative action by substituting what it considers to be a more adequate or proper basis." *Securities & Exchange Comm'n v. Chenery Corp.*, 332 U.S. 194, 196 (1947). As reiterated in *Federal Election Comm'n v. Akins*, 524 U.S. 11, 25 (1998), "If a reviewing court agrees that the agency misinterpreted the law, it will set aside the agency's action and remand the case — even though the agency (like a new jury after a mistrial) might later, in the exercise of its lawful discretion, reach the same result for a different reason." Thus we decline to consider alternative grounds that might support the Board's decision.

Further Proceedings

Sound administrative procedure requires that the agency apply the law in accordance with statute and precedent. The agency tribunal must make findings of relevant facts, and present its reasoning in sufficient detail that the court may conduct meaningful review of the agency action. In *Radio-Television News Directors Ass'n v. FCC*, 184 F.3d 872 (D.C.

Cir. 1999) the court discussed the "fine line between agency reasoning that is 'so crippled as to be unlawful' and action that is potentially lawful but insufficiently or inappropriately explained," quoting from *Checkosky v. Securities & Exch. Comm'n*, 23 F.3d 452, 464 (D.C. Cir. 1994); the court explained that "[i]n the former circumstance, the court's practice is to vacate the agency's order, while in the latter the court frequently remands for further explanation (including discussion of the relevant factors and precedents) while withholding judgment on the lawfulness of the agency's proposed action." *Id.* at 888. In this case the Board's analysis of the Lee invention does not comport with either the legal requirements for determination of obviousness or with the requirements of the Administrative Procedure Act that the agency tribunal set forth the findings and explanations needed for "reasoned decisionmaking." Remand for these purposes is required. *See Overton Park*, 401 U.S. at 420-221 (remanding for further proceedings appropriate to the administrative process).

VACATED AND REMANDED

Barbour v. Head

U.S. District Court
Southern District of Texas
No. G-01-491
Decided December 21, 2001

COPYRIGHTS

[1] Non-copyrightable matter — Ideas and systems (§ 211.05)

Defendants are not entitled to summary judgment that plaintiffs' cooking recipes are uncopyrightable, even though 17 U.S.C. § 102(b) denies copyright protection to mere procedures or processes, since neither courts nor Register of Copyrights have declared that recipes are per se uncopyrightable, since defendants have not shown that plaintiffs' cookbook is copyrighted as factual compilation or collective work rather than literary work, and since even if book is not literary work, genuine issue of material fact exists as to whether plaintiffs' recipes, which contain more than mechanical listings of ingredients and cooking instructions, represent mere unprotected facts or protectable expression.

JUDICIAL PRACTICE AND PROCEDURE

[2] Procedure — Limitations period; timeliness (§ 410.05)

Plaintiffs' claim for copyright infringement is not barred by three-year statute of limitations specified by 17 U.S.C. § 507(b), even though infringement claim was brought more than three years after infringing work was first published, since discovery rule and other equitable tolling doctrines apply to copyright claims, since plaintiffs' cause of action arguably did not accrue until they discovered defendants' book, less than one year before suit was brought, and since even if claim accrued on date of first publication, limitations period bars only remedy, not substantive right.

Action by Judy Barbour and Cookbook Resources LLC against James Head and Penfield Press Inc. for copyright infringement, and for unfair competition through misappropriation and conversion. On defendants' motion for summary judgment. Denied as to copyright claims; granted as to state law claims.

G.P. Hardy III, Houston, Texas, for plaintiffs.

Karen Bryant Tripp, Houston, for defendants.

Kent, J.

ORDER GRANTING IN PART DEFENDANT PENFIELD PRESS' MOTION TO DISMISS

This case involves a rustled cowboy cookbook. On August 13, 2001, Plaintiffs Judy Barbour ("Barbour") and Cookbook Resources, L.L.C. ("Cookbook Resources") filed causes of action for copyright infringement, unfair competition through misappropriation, and conversion, with which they're fixin' to brand Defendants James Head ("Head") and Penfield Press, Inc. ("Penfield Press"). On October 25, 2001, to bust out of the corral, Defendant Penfield Press filed a Motion to Dismiss pursuant to Fed.R.Civ.P. 12(b)(6). For the reasons articulated below, Defendant's Motion to Dismiss shall be

signs was not legally erroneous, and because we find that the Board's finding that Valu's guide rails are *de jure* functional is supported by substantial evidence, the Board's refusal to register Valu's guide rail designs is *affirmed*, and Rexnord's cross-appeal is dismissed as moot.

AFFIRMED

COSTS

No costs.

In re Lee

U.S. Court of Appeals
Federal Circuit

No. 00-1158

Decided January 18, 2002

PATENTS

[1] Practice and procedure in Patent and Trademark Office — Board of Patent Appeals and Interferences — In general (§ 110.1101)

Patentability/Validity — Obviousness — Combining references (§ 115.0905)

Patentability/Validity — Obviousness — Evidence of (§ 115.0906)

Rejection of patent application for obviousness under 35 U.S.C. § 103 must be based on evidence comprehended by language of that section, and search for and analysis of prior art includes evidence relevant to finding of whether there is teaching, motivation, or suggestion to select and combine references relied on as evidence of obviousness; factual inquiry whether to combine references must be thorough and searching, based on objective evidence of record, and Board of Patent Appeals and Interferences must explain reasons why one of ordinary skill in art would have been motivated to select references and to combine them to render claimed invention obvious.

[2] Patentability/Validity — Obviousness — Combining references (§ 115.0905)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

Board of Patent Appeals and Interferences improperly relied upon "common knowledge and common sense" of person of ordinary skill in art to find invention of patent application obvious over combination of two prior art references, since factual question of motivation to select and combine references is material to patentability, and could not be resolved on subjective belief and unknown authority, since deferential review of agency decisions under Administrative Procedure Act reinforces obligation of board to develop evidentiary basis for its findings, since board's rejection of need for any specific hint or suggestion in particular reference to support combination constituted omission of relevant factor required by precedent, and thus was both legal error and arbitrary agency action, since board's findings must extend to all material facts and be documented on record, and since "common knowledge and common sense" are not specialized knowledge and expertise of agency contemplated by APA, and may not be substituted for evidence, although they may be applied to analysis of evidence.

PATENTS

[3] Practice and procedure in Patent and Trademark Office — Board of Patent Appeals and Interferences — In general (§ 110.1101)

Patentability/Validity — Obviousness — Evidence of (§ 115.0906)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

Patent examiners and Board of Patent Appeals and Interferences, in relying on what they assert to be general knowledge to negate patentability on ground of obviousness, must articulate that knowledge and place it on record, since examiners and board are pre-

sumed to act from viewpoint of person of ordinary skill in art in finding relevant facts, assessing significance of prior art, and making ultimate determination of obviousness issue; failure to do so is not consistent with either effective administrative procedure or effective judicial review, and board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth rationale on which it relies.

[4] Procedure — Court of Appeals for the Federal Circuit (§ 410.03)

Procedure — Judicial review — Standard of review — Patents (§ 410.4607.09)

U.S. Court of Appeals for the Federal Circuit will not consider proposed alternative grounds for affirming decision of Board of Patent Appeals and Interferences rejecting patent application for obviousness, since alternative grounds were made at oral argument and constitute post hoc rationalization for agency action, consideration of which would deprive aggrieved party of fair opportunity to support its position.

Appeal from the U.S. Patent and Trademark Office, Board of Patent Appeals and Interferences.

Patent application of Sang-Su Lee, serial no. 07/631,210, directed to method of automatically displaying functions of video display device and demonstrating how to select and adjust functions to facilitate user response. Applicant appeals from decision upholding rejection of all claims for obviousness, and from reaffirmation of that decision on reconsideration. Reversed and remanded.

Richard H. Stern and Robert E. Bushnell, Washington, D.C., for Sang Su Lee.

Sidney O. Johnson Jr., associate solicitor, John M. Whealan, solicitor, and Raymond T. Chen, Maximilian R. Peterson, and Mark Nagumo, associate solicitors, Arlington, Va., for Director of U.S. Patent and Trademark Office.

Before Newman, Clevenger, and Dyk, circuit judges.

Newman, J.

Sang-Su Lee appeals the decision of the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office, rejecting all of the claims of Lee's patent application Serial No. 07/631,210 entitled "Self-Diagnosis and Sequential-Display Method of Every Function." [1] We vacate the Board's decision for failure to meet the adjudicative standards for review under the Administrative Procedure Act, and remand for further proceedings.

The Prosecution Record

Mr. Lee's patent application is directed to a method of automatically displaying the functions of a video display device and demonstrating how to select and adjust the functions in order to facilitate response by the user. The display and demonstration are achieved using computer-managed electronics, including pulse-width modulation and auto-fine-tuning pulses, in accordance with procedures described in the specification. Claim 10 is representative:

> 10. A method for automatically displaying functions of a video display device, comprising:
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> determining if a demonstration mode is selected;
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> if said demonstration mode is selected, automatically entering a picture adjustment mode having a picture menu screen displaying a list of a plurality of picture functions; and
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The examiner rejected the claims on the ground of obviousness, citing the combination of two references: United States Patent No. 4,626,892 to Nortrup, and the Thunderchopper Helicopter Operations Handbook for a video game. The Nortrup reference describes a television set having a menu display by which the user can adjust various picture and audio functions; however, the Nortrup display does not include a demonstration of how to adjust the functions. The Thunderchopper Handbook describes the Thunderchopper game's video display as having a "demonstration mode" showing how to play the game; however, the Thunderchopper Handbook makes no mention of the adjustment of picture or audio functions. The examiner held that it

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would have been obvious to a person of ordinary skill to combine the teachings of these references to produce the Lee system.

Lee appealed to the Board, arguing that the Thunderchopper Handbook simply explained how to play the Thunderchopper game, and that the prior art provided no teaching or motivation or suggestion to combine this reference with Nortrup, or that such combination would produce the Lee invention. The Board held that it was not necessary to present a source of a teaching, suggestion, or motivation to combine these references or their teachings. The Board stated:

> The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference.

Board op. at 7. The Board did not explain the "common knowledge and common sense" on which it relied for its conclusion that "the combined teachings of Nortrup and Thunderchopper would have suggested the claimed invention to those of ordinary skill in the art."

Lee filed a request for reconsideration, to which the Board responded after five years. The Board reaffirmed its decision, stating that the Thunderchopper Handbook was "analogous art" because it was "from the same field of endeavor" as the Lee invention, and that the field of video games was "reasonably pertinent" to the problem of adjusting display functions because the Thunderchopper Handbook showed video demonstrations of the "features" of the game. On the matter of motivation to combine the Nortrup and Thunderchopper references, the Board stated that "we maintain the position that we stated in our prior decision" and that the Examiner's Answer provided "a well reasoned discussion of why there is sufficient motivation to combine the references." The Board did not state the examiner's reasoning, and review of the Examiner's Answer reveals that the examiner merely stated that both the Nortrup function menu and the Thunderchopper demonstration mode are program features and that the Thunderchopper mode "is user-friendly" and it functions as a tutorial, and that it would have been obvious to combine them.

Lee had pressed the examiner during prosecution for some teaching, suggestion, or motivation in the prior art to select and combine the references that were relied on to show obviousness. The Examiner's Answer before the Board, plus a Supplemental Answer, stated that the combination of Thunderchopper with Nortrup "would have been obvious to one of ordinary skill in the art since the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software," and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial." The Board adopted the examiner's answer, stating "the examiner has provided a well reasoned discussion of these references and how the combination of these references meets the claim limitations." However, perhaps recognizing that the examiner had provided insufficient justification to support combining the Nortrup and Thunderchopper references, the Board held, as stated *supra*, that a "specific hint or suggestion" of motivation to combine was not required.

This appeal followed.

Judicial Review

Tribunals of the PTO are governed by the Administrative Procedure Act, and their rulings receive the same judicial deference as do tribunals of other administrative agencies. *Dickinson v. Zurko*, 527 U.S. 150, 50 USPQ2d 1930 (1999). Thus on appeal we review a PTO Board's findings and conclusions in accordance with the following criteria:

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> (2) hold unlawful and set aside agency actions, findings, and conclusions found to be—
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> (A) arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law;
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> (E) unsupported by substantial evidence in a case subject to sections 556 and 557 of this title or otherwise reviewed on the record of an agency hearing provided by statute;

For judicial review to be meaningfully achieved within these strictures, the agency tribunal must present a full and reasoned explanation of its decision. The agency tribunal

must set forth its findings and the grounds thereof, as supported by the agency record, and explain its application of the law to the found facts. The Court has often explained:

> The Administrative Procedure Act, which governs the proceedings of administrative agencies and related judicial review, establishes a scheme of "reasoned decisionmaking." Not only must an agency's decreed result be within the scope of its lawful authority, but the process by which it reaches that result must be logical and rational.

Allentown Mack Sales and Service, Inc. v. National Labor Relations Bd., 522 U.S. 359, 374 (1998) (citation omitted). This standard requires that the agency not only have reached a sound decision, but have articulated the reasons for that decision. The reviewing court is thus enabled to perform meaningful review within the strictures of the APA, for the court will have a basis on which to determine "whether the decision was based on the relevant factors and whether there has been a clear error of judgment." *Citizens to Preserve Overton Park v. Volpe*, 401 U.S. 402, 416 (1971). Judicial review of a Board decision denying an application for patent is thus founded on the obligation of the agency to make the necessary findings and to provide an administrative record showing the evidence on which the findings are based, accompanied by the agency's reasoning in reaching its conclusions. *See In re Zurko*, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) (review is on the administrative record); *In re Gartside*, 203 F.3d 1305, 1314, 53 USPQ2d 1769, 1774 (Fed. Cir. 2000) (Board decision "must be justified within the four corners of the record").

[1] As applied to the determination of patentability *vel non* when the issue is obviousness, "it is fundamental that rejections under 35 U.S.C. § 103 must be based on evidence comprehended by the language of that section." *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ 769, 775 (Fed. Cir. 1983). The essential factual evidence on the issue of obviousness is set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966) and extensive ensuing precedent. The patent examination process centers on prior art and the analysis thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. *See, e.g., McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the *Graham* factors).

"The factual inquiry whether to combine references must be thorough and searching." *Id.* It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. *See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding' ") (quoting *C.R. Bard, Inc., v. M3 Systems, Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (" 'teachings of references can be combined *only* if there is some suggestion or incentive to do so.' ") (emphasis in original) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).

The need for specificity pervades this authority. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combina-

tion. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); *In re Fritch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

[2] With respect to Lee's application, neither the examiner nor the Board adequately supported the selection and combination of the Nortrup and Thunderchopper references to render obvious that which Lee described. The examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Thus the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion.

Deferential judicial review under the Administrative Procedure Act does not relieve the agency of its obligation to develop an evidentiary basis for its findings. To the contrary, the Administrative Procedure Act reinforces this obligation. *See, e.g., Motor Vehicle Manufacturers Ass'n v. State Farm Mutual Automobile Ins. Co.*, 463 U.S. 29, 43 (1983) ("the agency must examine the relevant data and articulate a satisfactory explanation for its action including a 'rational connection between the facts found and the choice made.' ") (quoting *Burlington Truck Lines v. United States*, 371 U.S. 156, 168 (1962)); *Securities & Exchange Comm'n v. Chenery Corp.*, 318 U.S. 80, 94 (1943) ("The orderly function of the process of review requires that the grounds upon which the administrative agency acted are clearly disclosed and adequately sustained.").

In its decision on Lee's patent application, the Board rejected the need for "any specific hint or suggestion in a particular reference" to support the combination of the Nortrup and Thunderchopper references. Omission of a relevant factor required by precedent is both legal error and arbitrary agency action. *See Motor Vehicle Manufacturers*, 463 U.S. at 43 ("an agency rule would be arbitrary and capricious if the agency . . . entirely failed to consider an important aspect of the problem"); *Mullins v. Department of Energy*, 50 F.3d 990, 992 (Fed. Cir. 1995) ("It is well established that agencies have a duty to provide reviewing courts with a sufficient explanation for their decisions so that those decisions may be judged against the relevant statutory standards, and that failure to provide such an explanation is grounds for striking down the action."). As discussed in *National Labor Relations Bd. v. Ashkenazy Property Mgt. Corp.*, 817 F.2d 74, 75 (9th Cir. 1987), an agency is "not free to refuse to follow circuit precedent."

The foundation of the principle of judicial deference to the rulings of agency tribunals is that the tribunal has specialized knowledge and expertise, such that when reasoned findings are made, a reviewing court may confidently defer to the agency's application of its knowledge in its area of expertise. Reasoned findings are critical to the performance of agency functions and judicial reliance on agency competence. *See Baltimore and Ohio R. R. Co. v. Aberdeen & Rockfish R. R. Co.*, 393 U.S. 87, 91-92 (1968) (absent reasoned findings based on substantial evidence effective review would become lost "in the haze of so-called expertise"). The "common knowledge and common sense" on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation. This court explained in *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697, that "deficiencies of the cited references cannot be remedied by

the Board's general conclusions about what is 'basic knowledge' or 'common sense.' " The Board's findings must extend to all material facts and must be documented on the record, lest the "haze of so-called expertise" acquire insulation from accountability. "Common knowledge and common sense," even if assumed to derive from the agency's expertise, do not substitute for authority when the law requires authority. *See Allentown Mack*, 522 U.S. at 376 ("Because reasoned decisionmaking demands it, and because the systemic consequences of any other approach are unacceptable, the Board must be required to apply in fact the clearly understood legal standards that it enunciates in principle . . . .")

The case on which the Board relies for its departure from precedent, *In re Bozek*, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969), indeed mentions "common knowledge and common sense," the CCPA stating that the phrase was used by the Solicitor to support the Board's conclusion of obviousness based on evidence in the prior art. *Bozek* did not hold that common knowledge and common sense are a substitute for evidence, but only that they may be applied to analysis of the evidence. *Bozek* did not hold that objective analysis, proper authority, and reasoned findings can be omitted from Board decisions. Nor does *Bozek*, after thirty-two years of isolation, outweigh the dozens of rulings of the Federal Circuit and the Court of Customs and Patent Appeals that determination of patentability must be based on evidence. This court has remarked, in *Smiths Industries Medical Systems, Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1356, 51 USPQ2d 1415, 1421 (Fed. Cir. 1999), that *Bozek*'s reference to common knowledge "does not in and of itself make it so" absent evidence of such knowledge.

[3] The determination of patentability on the ground of unobviousness is ultimately one of judgment. In furtherance of the judgmental process, the patent examination procedure serves both to find, and to place on the official record, that which has been considered with respect to patentability. The patent examiner and the Board are deemed to have experience in the field of the invention; however, this experience, insofar as applied to the determination of patentability, must be applied from the viewpoint of "the person having ordinary skill in the art to which said subject matter pertains," the words of section 103. In finding the relevant facts, in assessing the significance of the prior art, and in making the ultimate determination of the issue of obviousness, the examiner and the Board are presumed to act from this viewpoint. Thus when they rely on what they assert to be general knowledge to negate patentability, that knowledge must be articulated and placed on the record. The failure to do so is not consistent with either effective administrative procedure or effective judicial review. The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies.

Alternative Grounds

[4] At oral argument the PTO Solicitor proposed alternative grounds on which this court might affirm the Board's decision. However, as stated in *Burlington Truck Lines, Inc. v. United States*, 371 U.S. 156, 168 (1962), "courts may not accept appellate counsel's *post hoc* rationalization for agency action." Consideration by the appellate tribunal of new agency justifications deprives the aggrieved party of a fair opportunity to support its position; thus review of an administrative decision must be made on the grounds relied on by the agency. "If those grounds are inadequate or improper, the court is powerless to affirm the administrative action by substituting what it considers to be a more adequate or proper basis." *Securities & Exchange Comm'n v. Chenery Corp.*, 332 U.S. 194, 196 (1947). As reiterated in *Federal Election Comm'n v. Akins*, 524 U.S. 11, 25 (1998), "If a reviewing court agrees that the agency misinterpreted the law, it will set aside the agency's action and remand the case — even though the agency (like a new jury after a mistrial) might later, in the exercise of its lawful discretion, reach the same result for a different reason." Thus we decline to consider alternative grounds that might support the Board's decision.

Further Proceedings

Sound administrative procedure requires that the agency apply the law in accordance with statute and precedent. The agency tribunal must make findings of relevant facts, and present its reasoning in sufficient detail that the court may conduct meaningful review of the agency action. In *Radio-Television News Directors Ass'n v. FCC*, 184 F.3d 872 (D.C.

Cir. 1999) the court discussed the "fine line between agency reasoning that is 'so crippled as to be unlawful' and action that is potentially lawful but insufficiently or inappropriately explained," quoting from *Checkosky v. Securities & Exch. Comm'n*, 23 F.3d 452, 464 (D.C. Cir. 1994); the court explained that "[i]n the former circumstance, the court's practice is to vacate the agency's order, while in the latter the court frequently remands for further explanation (including discussion of the relevant factors and precedents) while withholding judgment on the lawfulness of the agency's proposed action." *Id.* at 888. In this case the Board's analysis of the Lee invention does not comport with either the legal requirements for determination of obviousness or with the requirements of the Administrative Procedure Act that the agency tribunal set forth the findings and explanations needed for "reasoned decisionmaking." Remand for these purposes is required. *See Overton Park*, 401 U.S. at 420-221 (remanding for further proceedings appropriate to the administrative process).

VACATED AND REMANDED

Barbour v. Head

U.S. District Court
Southern District of Texas

No. G-01-491

Decided December 21, 2001

COPYRIGHTS

[1] Non-copyrightable matter — Ideas and systems (§ 211.05)

Defendants are not entitled to summary judgment that plaintiffs' cooking recipes are uncopyrightable, even though 17 U.S.C. § 102(b) denies copyright protection to mere procedures or processes, since neither courts nor Register of Copyrights have declared that recipes are per se uncopyrightable, since defendants have not shown that plaintiffs' cookbook is copyrighted as factual compilation or collective work rather than literary work, and since even if book is not literary work, genuine issue of material fact exists as to whether plaintiffs' recipes, which contain more than mechanical listings of ingredients and cooking instructions, represent mere unprotected facts or protectable expression.

JUDICIAL PRACTICE AND PROCEDURE

[2] Procedure — Limitations period; timeliness (§ 410.05)

Plaintiffs' claim for copyright infringement is not barred by three-year statute of limitations specified by 17 U.S.C. § 507(b), even though infringement claim was brought more than three years after infringing work was first published, since discovery rule and other equitable tolling doctrines apply to copyright claims, since plaintiffs' cause of action arguably did not accrue until they discovered defendants' book, less than one year before suit was brought, and since even if claim accrued on date of first publication, limitations period bars only remedy, not substantive right.

Action by Judy Barbour and Cookbook Resources LLC against James Head and Penfield Press Inc. for copyright infringement, and for unfair competition through misappropriation and conversion. On defendants' motion for summary judgment. Denied as to copyright claims; granted as to state law claims.

G.P. Hardy III, Houston, Texas, for plaintiffs.

Karen Bryant Tripp, Houston, for defendants.

Kent, J.

ORDER GRANTING IN PART DEFENDANT PENFIELD PRESS' MOTION TO DISMISS

This case involves a rustled cowboy cookbook. On August 13, 2001, Plaintiffs Judy Barbour ("Barbour") and Cookbook Resources, L.L.C. ("Cookbook Resources") filed causes of action for copyright infringement, unfair competition through misappropriation, and conversion, with which they're fixin' to brand Defendants James Head ("Head") and Penfield Press, Inc. ("Penfield Press"). On October 25, 2001, to bust out of the corral, Defendant Penfield Press filed a Motion to Dismiss pursuant to Fed.R.Civ.P. 12(b)(6). For the reasons articulated below, Defendant's Motion to Dismiss shall be